7I95T
ETHERNET STEP/DIR + ENCODER MOTION CONTROL INTERFACE

V1.0

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GENERAL

DESCRIPTION

The 7I95T is a Ethernet connected motion control interface designed for interfacing up to 6 Axis of step&dir step motor or servo motor drives and includes encoder feedback for each axis. Step rates up to 10 MHz are supported. The 7I95T also has 24 isolated inputs plus 6 isolated outputs for general purpose I/O use. 6 high speed encoder interfaces are provided axis feedback and for spindle synchronized motion. Two RS-422/RS485 serial expansion ports and a parallel expansion port are also provided.

All step and direction outputs are buffered 5V signals that can drive 24 mA. All outputs support differential mode to reduce susceptibility to noise. The encoders can be used with TTL or differential input.

24 isolated inputs are provided for general control use including limit switch and control panel inputs. Inputs operate with 4V to 36V DC and can have a positive or negative common for sourcing or sinking input applications. 8 of the isolated inputs can be used to support up to 4 quadrature MPGs. Six 36V 2A isolated outputs allow sinking, sourcing combinations of both.

Two RS-422/RS-485 interface is provided for I/O expansion via a serial I/O daughtercard. In addition to the on card I/O, A FPGA expansion connector compatible with Mesa's 25 pin daughtercards or standard parallel port breakout boards allow almost unlimited I/O options including additional quadrature or absolute encoder inputs, step/dir or PWM/dir outputs, and field I/O expansion to hundreds of I/O points. All field wiring is terminated in pluggable 3.5 mm screw terminal blocks. The 7I95T runs from a single 5V supply

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I95T card is oriented in an upright position, that is, with the host interface RJ-45 connector pointing towards the left.

ENCODER INPUT MODES

The 7I95Ts six encoder inputs can be programmed for differential or single ended mode operation. Each encoder has 3 jumpers which set the input mode of the individual A/B/Z inputs. Normally these jumper will all be set to single ended or differential on a single encoder channel. The jumpers are set to the right hand position for differential inputs and the left hand position for single ended inputs. Note that the groups of three jumpers are close to the associated encoder connector. Default setting is differential (right hand position) for all encoders.

ENCODER	A	B	Z
0	W21	W19	W13
1	W11	W9	W7
2	W5	W3	W1
3	W22	W20	W14
4	W12	W10	W8
5	W6	W4	W2

HARDWARE CONFIGURATION

EXPANSION CONNECTOR 5V POWER

The 7I95T has the option to supply 5V power to the breakout board connected to its expansion connector (P1).

This option should only be enabled for Mesa breakout boards or boards specifically wired to accept 5V power on DB25 pins 22 through 25. When the option is disabled DB25 pins 22 through 25 are grounded. Jumper W23 controls the breakout power option.

JUMPER	POS	FUNCTION
W18	UP	5V BREAKOUT POWER ON
W18	DOWN	5V BREAKOUT POWER OFF (*DEFAULT*)

P1 PULLUP/PULLDOWN OPTION

P1 I/O pins have the option of being pulled up to 5V or pulled down to ground via 4.7K resistors. This is important as it defines the pin states when the board is first powered up or when a watchdog bite occurs.

JUMPER	POS	FUNCTION
W17	UP	ALL P1 PINS PULLED UP TO 5V
W17	DOWN	ALL P1 PINS PULLED DOWN TO GND

HARDWARE CONFIGURATION

IP ADDRESS SELECTION

The 7I95T has three options for selecting its IP address. These options are selected by Jumpers W15 and W16.

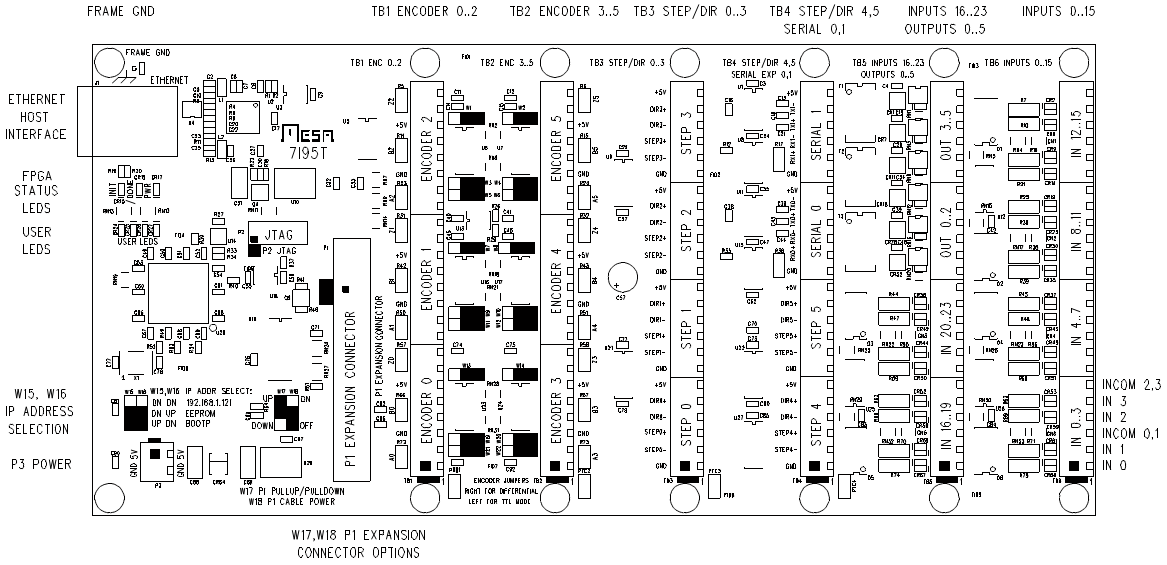
W15	W16	IP ADDRESS	
DOWN	DOWN	FIXED 192.168.1.121	(DEFAULT)
DOWN	UP	FIXED FROM EEPROM	
UP	DOWN	BOOTP	
UP	UP	FIXED 192.168.1.121 + FORCE FALLBACK BOOT	

Note: The as shipped default EEPROM IP address is 10.10.10.10. This can be changed via the mesaflash utility

CONNECTORS

7I95T CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS

NOTE: BLACK SQUARES INDICATE PIN 1



CONNECTORS

P3 POWER CONNECTOR PINOUT

P3 is the 7I95Ts 5V power connector. ***Do not supply any voltage other than 5V to P3!*** P3 is a 3.5MM plug-in screw terminal block. P3 pinout is as follows:

PIN	FUNCTION	
1	+5V	TOP, SQUARE PAD
2	GND	BOTTOM, ROUND PAD

P2 JTAG CONNECTOR PINOUT

P2 is a JTAG programming connector. This is normally used only for debugging or if both user and fallback EEPROM configurations have been corrupted. In case of corrupted EEPROM contents the EEPROM can be re-programmed using Efinix's stand alone programming tool.

P2 JTAG CONNECTOR PINOUT

PIN	FUNCTION	PIN	FUNCTION
1	TMS	2	TDI
3	TDO	4	GND
5	TCK	6	GND
7	/RESET	8	GND
9	/SS	10	+3.3V

FRAME GROUND

The top left mounting hole (near the Ethernet jack) is the frame ground connection. This should be grounded to earth/frame ground for best ESD/EMI resistance

CONNECTORS

P1 EXPANSION CONNECTOR

The 7I95T has a 26 pin header to allow I/O expansion beyond the built in I/O on the 7I95T card. This I/O can include more step/dir channels, encoders, etc. This header has a pin-out that matches standard parallel port breakout cards and Mesa's 25 pin FPGA daughtercards, when terminated with a DB25 connector.

P1 PIN	DB25 PIN	P1 FUNC	P1 PIN	DB25 PIN	P1 FUNC
1	1	IO41	2	14	IO42
3	2	IO43	4	15	IO44
5	3	IO45	6	16	IO46
7	4	IO47	8	17	IO48
9	5	IO49	10	18	GND
11	6	IO50	12	19	GND
13	7	IO51	14	20	GND
15	8	IO52	16	21	GND
17	9	IO53	18	22	GND / 5V
19	10	IO54	20	23	GND / 5V
21	11	IO55	22	24	GND or 5V
23	12	IO56	24	25	GND or 5V
25	13	IO57	26	XX	GND or 5V

P1 header pins 18,20,22,24,26 (DB25 pins 22 through 25) can be tied to ground or 5V, depending on W18 position.

CONNECTORS

TB1 ENCODER 0..2 CONNECTOR

TB1 is the 7I95Ts encoder 0 through 2 connector. Each encoder interface uses 8 pins TB1 is a 24 pin 3.5 MM pluggable terminal block with supplied with three eight pin removable screw terminal plugs.

TB1 PIN	FUNCTION	DIR
1	QA0	TO 7I95T
2	/QA0	TO 7I95T
3	GND	FROM 7I95T
4	QB0	TO 7I95T
5	/QB0	TO 7I95T
6	+5V	FROM 7I95T
7	IDX0	TO 7I95T
8	/IDX0	TO 7I95T
9	QA1	TO 7I95T
10	/QA1	TO 7I95T
11	GND	FROM 7I95T
12	QB1	TO 7I95T
13	/QB1	TO 7I95T
14	+5V	FROM 7I95T
15	IDX1	TO 7I95T
16	/IDX1	TO 7I95T
17	QA2	TO 7I95T
18	/QA2	TO 7I95T
19	GND	FROM 7I95T
20	QB2	TO 7I95T
21	/QB2	TO 7I95T
22	+5V	FROM 7I95T
23	IDX2	TO 7I95T
24	/IDX2	TO 7I95T

CONNECTORS

TB2 ENCODER 3..5 CONNECTOR

TB2 is the 7I95Ts encoder 3 through 5 connector. Each encoder interface uses 8 pins. TB2 is a 24 pin 3.5 MM pluggable terminal block supplied with three eight pin removable screw terminal plugs.

TB2 PIN	FUNCTION	DIR
1	QA3	TO 7I95T
2	/QA3	TO 7I95T
3	GND	FROM 7I95T
4	QB3	TO 7I95T
5	/QB3	TO 7I95T
6	+5V	FROM 7I95T
7	IDX3	TO 7I95T
8	/IDX3	TO 7I95T
9	QA4	TO 7I95T
10	/QA4	TO 7I95T
11	GND	FROM 7I95T
12	QB4	TO 7I95T
13	/QB4	TO 7I95T
14	+5V	FROM 7I95T
15	IDX4	TO 7I95T
16	/IDX4	TO 7I95T
17	QA5	TO 7I95T
18	/QA5	TO 7I95T
19	GND	FROM 7I95T
20	QB5	TO 7I95T
21	/QB5	TO 7I95T
22	+5V	FROM 7I95T
23	IDX5	TO 7I95T
24	/IDX5	TO 7I95T

CONNECTORS

TB3 STEP/DIR 0..3 CONNECTOR

TB3 is the 7I95Ts main step and direction output connector. Both polarities of step and direction signals are provided. Each channel on the interface uses 6 pins. TB3 is a 3.5 MM pluggable terminal block with supplied removable screw terminal plugs.

TB3 CONNECTOR PINOUT

TB3 PIN	SIGNAL	TB3 PIN	SIGNAL
1	GND	13	GND
2	STEP0-	14	STEP2-
3	STEP0+	15	STEP2+
4	DIR0-	16	DIR2-
5	DIR0+	17	DIR2+
6	+5VP	18	+5VP
7	GND	19	GND
8	STEP1-	20	STEP3-
9	STEP1+	21	STEP3+
10	DIR1-	22	DIR3-
11	DIR1+	23	DIR3+
12	+5VP	24	+5VP

Note: 5VP pins are PTC short circuit protected 5V output pins for field wiring.

CONNECTORS

TB4 STEP/DIR 4,5, SERIAL EXPANSION CONNECTOR

TB4 has a mix of signals including step/dir channel 4, an encoder interface, a RS-422/485 interface, and 5V logic supply power input. TB4 is a 24 terminal 3.5 MM pluggable terminal block with supplied removable screw terminal plugs.

TB4 CONNECTOR PINOUT

TB4 PIN	SIGNAL	TB4 PIN	SIGNAL
1	GND	13	GND
2	STEP4-	14	RS-422/485 RX0+
3	STEP4+	15	RS-422/485 RX0-
4	DIR4-	16	RS-422 /485 TX0+
5	DIR4+	17	RS-422/485 TX0-
6	+5VP	18	+5VP
7	GND	19	GND
8	STEP5-	20	RS-422/485 RX1+
9	STEP5+	21	RS-422/485 RX1-
10	DIR5-	22	RS-422/485 TX1+
11	DIR5+	23	RS-422/485 TX1-
12	+5VP	24	+5VP

Note: 5VP pins are PTC short circuit protected 5V output pins for field wiring.

CONNECTORS

TB5 ISOLATED I/O CONNECTOR

Terminal block TB5 is one the 7I95Ts isolated I/O connectors. This has 8 inputs (16 through 23)and six isolated high current outputs.

TB5 CONNECTOR PINOUT

TB5 PIN	I/O	TB5 PIN	I/O
1	INPUT16	13	OUT0-
2	INPUT17	14	OUT0+
3	INCOM16,17	15	OUT1-
4	INPUT18	16	OUT1+
5	INPUT19	17	OUT2-
6	INCOM18,19	18	OUT2+
7	INPUT20	19	OUT3-
8	INPUT21	20	OUT3+
9	INCOM20,21	21	OUT4-
10	INPUT22	22	OUT4+
11	INPUT23	23	OUT5-
12	INCOM22.23	24	OUT5+

CONNECTORS

TB6 ISOLATED INPUT CONNECTOR

Terminal block TB6 is one the 7I95Ts isolated I/O connectors. This has 16 inputs (0 through 15)

TB6 CONNECTOR PINOUT

TB6 PIN	I/O	TB6 PIN	I/O
1	INPUT0	13	INPUT8
2	INPUT1	14	INPUT9
3	INCOM0,1	15	INCOM8,9
4	INPUT2	16	INPUT10
5	INPUT3	17	INPUT11
6	INCOM2,3	18	INCOM10,11
7	INPUT4	19	INPUT12
8	INPUT5	20	INPUT13
9	INCOM4,5	21	INCOM12,13
10	INPUT6	22	INPUT14
11	INPUT7	23	INPUT15
12	INCOM6,7	24	INCOM14,15

OPERATION

RS-422/RS-485 INTERFACE

The 7I95T has two RS-422/RS-485 interfaces available on TB4. This interface is intended for I/O expansion with Mesa SSerial devices. The easiest way to make a cable for interfacing the 7I95T to these devices is to take a standard CAT5 or CAT6 cable, cut it in half, and wire the individual wires to the 7I95T screw terminals. The following chart gives the CAT5 to 7I95T screw terminal connections with EIA/TIA 568B colors:

TB4 PIN	SIGNAL	DIRECTION	CAT5 PIN	CAT5 568B COLOR
13,19	GND	FROM 7I95T	4,5	BLUE, BLUE / WHITE
14,20	RX+	TO 7I95T	6	GREEN
15,21	RX-	TO 7I95T	3	GREEN / WHITE
16,22	TX+	FROM 7I95T	2	ORANGE
17,23	TX-	FROM 7I95T	1	ORANGE / WHITE
18,24	+5V	FROM 7I95T	7,8	BROWN / WHITE,BROWN

Note: The 6 pin terminal block requires the +5V (brown and brown/white) and ground (blue and blue/white) pairs to be terminated in single screw terminal positions.

TB4 pins 13 through 18 are serial channel 0, TB4 pins 19 through 24 are serial channel 1

For 2 wire RS-485 applications, TX+ must be connected to RX+ and TX- must be connected to RX-.

OPERATION

STEP/DIR INTERFACE

The 7I95T provides six channels of step/dir interface with buffered 5V differential signal pairs. Each differential pair consists of two complementary 5V outputs. The differential signals allows reliable signal transmission in noisy environments and can directly interface with RS-422 line receivers. Step motor drives with single ended inputs connect to just one of the STEP and DIR signal outputs, that is either the STEP+/DIR+ or STEP-/DIR- signals, with the unused signals left unconnected at the 7I95T. The input common signal on drives with single ended inputs connects to the 7I95Ts GND or 5VP pins depending on the drive type.

ENCODER INTERFACE

The 7I95T provides six channels of quadrature encoder interface with index. Encoder inputs can be programmed for differential or single ended encoders. The encoder interface also provides short circuit protected 5V power to the encoders. When used with single ended encoders, the ENCA+, ENCB+ and IDX+ signals are wired to the encoder and the ENCA-,ENCB-, and IDX- terminal left unconnected.

MAXIMUM ENCODER COUNT RATE

The 7I975 uses multiplexed encoder signals to save FPGA pins. The multiplexing rate will determine the maximum encoder count rate. Default multiplexing rate with HostMot2 firmware is ClockLow /16,or approximately 6 MHz giving a resolvable count rate of 3 MHz.

OPERATION

BOARD STATUS LEDS

The 7I95T has seven LEDS for card status monitoring. The color, function and locations are as follows:

LED	COLOR	FUNCTION	OK	LOCATION
CR15	RED	FPGA /INIT	OFF	TOP LEFT
CR16	RED	FPGA /DONE	OFF	TOP LEFT
CR17	YELLOW	LOGIC POWER	ON	TOP LEFT
CR24	GREEN	USER LED3	ANY	TOP LEFT
CR25	GREEN	USER LED2	ANY	TOP LEFT
CR26	GREEN	USER LED1	ANY	TOP LEFT
CR27	GREEN	USER LED0	ANY	TOP LEFT

In normal operation CR15 and CR16 will be off. If either is on after power-up there is a problem with configuring the FPGA. **CR15 is also used to signal a HostMot2 watchdog bite so will be illuminated when LinuxCNC exits.** CR17 (power LED) will also be on. The user LEDs default function counts received packets but their function can be changed to user accessible HostMot2 LEDs if desired.

I/O STATUS LEDS

In addition to the board status LEDs, each isolated input and output has an associated yellow LED that illuminates when the input or output is active.

ISOLATED I/O

The 7I95T has 24 isolated inputs and 6 isolated outputs. All 24 Isolated inputs have a common pin per input pair. This common pin must be connected to ground for active high inputs and connected to the I/O power for active low inputs. The 6 isolated outputs are completely floating switches so can be use for pull-up/pull-down and mixed voltage switching.

OPERATION

ISOLATED INPUT CHARACTERISTICS

The isolated inputs use opto-isolators with a 4.7K input series resistance. This results in an approximate current draw of 5 mA at 24V. The inputs will operate with +-4V to +-36V signals relative to input common. Isolated inputs are relatively slow and not suited for signals faster than about 4 KHz. Each input pair has a separate common connection to allow mixing of sinking/sourcing and mixed supply voltages.

For PNP type sensors or switches with a common positive, the input common pin for a given input pair is grounded.

For NPN type sensors or switches with a common ground, the input common for a given input pair is connected to +5 to +36V and the input pins are grounded to activate an input.

MPG ENCODER INPUTS

Standard 7I95T firmware provides 4 quadrature MPG encoder inputs on isolated inputs 0 through 7. Since the input threshold on isolated inputs is about 3V, its best to use sinking inputs (with the input common terminal tied to +5V) with TTL output level MPGs.

INPUT	ENCODER	INPUT	ENCODER
0	QUADA-0	4	QUADA-2
1	QUADB-0	5	QUADB-2
2	QUADA-1	6	QUADA-3
3	QUADB-1	7	QUADB-3

ISOLATED OUTPUT CHARACTERISTICS

The 6 isolated outputs use full floating MOSFET switches (a DC Solid State Relay or SSR) and can be used just like a switch or relay contact. Maximum voltage is 36 VDC and maximum load current is 2A. Inductive loads must have a flyback diode. The output polarity must be observed (reversed outputs will be stuck-on).

Note: The 7I95T outputs are not short circuit protected so a current limited power supply or a 2A to 5A fuse should be used in the power source that supplies the outputs.

HOST INTERFACE

FPGA

The 7I95T use a Efinix Trion FPGA in a BGA256 package: T20F256C4.

IP ADDRESS SELECTION

Initial communication with the 7I95T requires knowing its IP address. The 7I95T has 3 IP address options: Default, EEPROM, and Bootp, selected by jumpers W5 and W6. Default IP address is always 192.168.1.121. The EEPROM IP address is set by writing Ethernet EEPROM locations 0x20 and 0X22. BootP allows the 7I95T address to be set by a DHCP/ BootP server. If BootP is chosen, the 7I95T will retry BootP requests at a ~1 Hz rate if the BootP server does not respond.

HOST COMMUNICATION

The 7I95T standard firmware is designed for low overhead real time communication with a host controller so implements a very simple set of IPV4 operations. These operations include ARP reply, ICMP echo reply, and UDP packet receive/send for host data communications. UDP is used so that the 7I95T can be used on a standard network with standard tools for non-real time applications. No fragmentation is allowed so maximum packet size is 1500 bytes.

UDP

All 7I95T Ethernet communication is done via UDP packets. The 7I95T socket number for UDP data communication is 27181. Read data is routed to the requesters port number. Under UDP, a simple register access protocol is used. This protocol is called LBP16.

LBP16

LBP16 allows read and write access to up to eight separate address spaces with different sizes and characteristics. Current firmware uses seven of these spaces. For efficiency, LBP16 allows access to blocks of registers at sequential increasing addresses. (Block transfers)

WINDOWS ARP ISSUES

The Windows XP and earlier TCP stack has a characteristic that causes it to drop outgoing UDP packets when refreshing its ARP cache. Because of this you must either verify packet transmission via echoing data from the 7I95T for every transaction (reading RXUDPCount is suggested) and retrying failed transactions, or alternatively, setting up a static entry for the 7I95T in the ARP table. This is done with windows ARP command.

HOST INTERFACE

CONFIGURATION

The 7I95T is configured at power up by a SPI FLASH memory. This flash memory is an 16M bit chip that has space for two configuration files. Since all Ethernet logic on the 7I95T is in the FPGA, a problem with configuration means that Ethernet access will not be possible. For this reason there is a backup method to recover from FPGA boot failures.

FALLBACK

The backup system is called Fallback. The 7I95T flash memory normally contains two configuration file images, A user image and a fallback image. If the primary user configuration is corrupted, the FPGA will load the fallback configuration so the flash memory image can be repaired remotely without having to resort JTAG programming.

Note that if you program the 7I95T with a valid bitfile for a T20F256 but not designed for a 7I95T, you will likely "brick" the card. If this happens, the first thing to try is setting the IP address select option jumpers to the UP,UP positions. This will force a boot from the fallback memory location, and should allow reprogramming of the user configuration. Note that the card IP address is fixed at 192.168.1.121 when the IP select jumpers are in the UP,UP setting.

HOST INTERFACE

EEPROM LAYOUT

The EEPROM used on the 7I95T for configuration storage is the M25P16. The M25P16 is a 16 M bit (2 M byte) EEPROM with 32 64K byte sectors. Configuration files are stored on sector boundaries to allow individual configuration file erasing and updating. Standard EEPROM sector layout is as follows:

0x000000	FALLBACK CONFIGURATION BLOCK 0
0x010000	FALLBACK CONFIGURATION BLOCK 1
0x020000	FALLBACK CONFIGURATION BLOCK 2
0x030000	FALLBACK CONFIGURATION BLOCK 3
0x040000	FALLBACK CONFIGURATION BLOCK 4
0x050000	FALLBACK CONFIGURATION BLOCK 5
0x060000	FALLBACK CONFIGURATION BLOCK 6
0x070000	FALLBACK CONFIGURATION BLOCK 7
0x080000	FALLBACK CONFIGURATION BLOCK 8
0x090000	FALLBACK CONFIGURATION BLOCK 9
0x0A0000	FALLBACK CONFIGURATION BLOCK 10
0x0B0000	UNUSED/FREE
0x0C0000	UNUSED/FREE
0x0D0000	UNUSED/FREE
0x0E0000	UNUSED/FREE
0x0F0000	UNUSED/FREE

HOST INTERFACE

EEPROM LAYOUT

0x100000	USER CONFIGURATION BLOCK 0
0x110000	USER CONFIGURATION BLOCK 1
0x120000	USER CONFIGURATION BLOCK 2
0x130000	USER CONFIGURATION BLOCK 3
0x140000	USER CONFIGURATION BLOCK 4
0x150000	USER CONFIGURATION BLOCK 5
0x160000	USER CONFIGURATION BLOCK 6
0x170000	USER CONFIGURATION BLOCK 7
0x180000	USER CONFIGURATION BLOCK 8
0x190000	USER CONFIGURATION BLOCK 9
0x1A0000	USER CONFIGURATION BLOCK 10
0x1B0000	UNUSED/FREE
0x1C0000	UNUSED/FREE
0x1D0000	UNUSED/FREE
0x1E0000	UNUSED/FREE
0x1F0000	UNUSED/FREE

HOST INTERFACE

BITFILE FORMAT

The configuration utilities expect standard FPGA bitfiles without any multiboot features enabled. If multiboot FPGA files are loaded they will likely cause a configuration failure. The fallback configuration must use 7i96s_16m_fallback.bin. *The fallback configuration should not be updated unless the configuration is corrupt, never write a user configuration to the fallback location nor a fallback configuration to the user location*.

MESAFLASH

Linux utility program mesaflash is provided to write configuration files to the 7I96S EEPROM. These files depend on a simple SPI interface built into both the standard user FPGA bitfiles and the fallback bitfile. *The MESAFLASH utilities expect standard FPGA bitfiles without any multiboot features enabled. If multiboot FPGA files are loaded they will likely cause a configuration failure. Mesaflash version 3.4.7 or greater is required to write bitfiles to the 7I95T.* ***DO NOT write 7I95 bitfiles to the 7I95S***

If mesaflash is run with a –help command line argument it will print usage information.

The following examples assume the target 7I95T is using the ROM IP address of 192.168.1.121.

`mesaflash --device 7I95T --addr 192.168.1.121 --write FPGAFILE.BIN`

Writes a FPGA configuration file: FPGAFILE.BIN to the user area of the EEPROM.

`mesaflash --device 7I95T --addr 192.168.1.121 --verify FPGAFILE.BIN`

Verifies the user EEPROM configuration against the bit file FPGAFILE.BIT.

SETTING EEPROM IP ADDRESS

mesaflash can also write the EEPROM IP address of the 7I95T:

`mesaflash --device 7I95T --addr 192,168,1,121 --set ip=192.168.0.100`

The above examples assume the 7I95T has its default ROM IP address (192.168.1.121)

HOST INTERFACE

FREE FLASH MEMORY SPACE

Ten 64K byte blocks of flash memory space are free when both user and fallback configurations are installed on the 7I95T. It is suggested that only the last two blocks, 0x1E0000 and 0x1F0000 in the user area, be used for FPGA application flash storage.

FALLBACK INDICATION

Mesa's supplied fallback configurations blink the red INIT LED on the top right hand side of the card if the primary configuration fails and the fallback configuration loaded successfully. If this happens it means the user configuration is corrupted or not a proper configuration for the 7I95Ts FPGA. This can be fixed by running the configuration utility and re-writing the user configuration**.**

FAILURE TO CONFIGURE

The 7I95T should configure its FPGA within a fraction of a second of power application. If the FPGA card fails to configure, the red /DONE LED CR2 will remain illuminated. If this happens, the first thing to try is setting the IP address select option jumpers to the UP,UP positions. This will force a boot from the fallback memory location, and should allow reprogramming of the user configuration. Note that the card IP address is fixed at 192.168.1.121 when the IP select jumpers are in the UP,UP setting. If this fails, the 7I95Ts EEPROM must be re-programmed via the JTAG connector or (faster) JTAG FPGA load followed by Ethernet EEPROM update.

CLOCK SIGNALS

The 7I95T has a single 50 MHz clock signal from an on card crystal oscillator. The clock a can be multiplied and divided by the FPGAs clock generator block to generate a wide range of internal clock signals. The 50 MHz clock is also used to generate the 25MHz clock for the Ethernet interface chip.

HOST INTERFACE

LOGIC POWER

5V logic power for the host interface FPGA, expansion connectors, RS-422 and encoder connections and step/dir connections can be provided at connector P3, or alternatively TB2.

P1 PULLUP/PULLDOWN RESISTORS

All P1 expansion I/O pins are provided with pull-up/pulldown resistors to allow connection to open drain, open collector, or OPTO devices and to set the power-up state of the pins. These resistors have a value of 4.7K so have a maximum pullup/pulldown current of ~1.07 mA at 5V.

EXPANSION CONNECTOR IO LEVELS

The Efinix FPGAs used on the 7I95T have programmable I/O levels for interfacing with different logic families. The 7I95T does not support use of the I/O standards that require input reference voltages. All standard Mesa configurations use LVTTL levels.

Note that even though the 7I95T expansion I/O can tolerate 5V signal inputs, its outputs will not swing to 5V. The outputs are push pull CMOS that will drive to the output supply rail of 3.3V. This is sufficient for TTL compatibility but may cause problems with some types of loads. For example when driving an LED that has its anode connected to 5V, in such devices as OPTO isolators and I/O module rack SSRs, the 3.3V high level may not completely turn the LED off. To avoid this problem, either drive loads that are ground referred, Use 3.3V as the VCC for VCC referred loads, or use open drain mode.

EXPANSION CONNECTOR STARTUP I/O VOLTAGE

After power-up or watchdog bite, the expansion connector pin states are determined by the pullup or pulldown resistors. If the expansion connector pins are used for motion control or controlling devices that could present a hazard when enabled, external circuitry should be designed so that this initial state results in a safe condition.

REFERENCE INFORMATION

LBP16

GENERAL

LBP16 is the simple register access protocol used by the 7I95T for all Ethernet communications.

LBP16 COMMANDS

LBP16 is a simple remote register access protocol to allow efficient register access over the Ethernet link. All LBP16 commands are 16 bits in length and have the following structure:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	A	C	M	M	M	S	S	I	N	N	N	N	N	N	N

W Is the write bit (1 means write, 0 means read)

A Is the includes Address bit. If this is '1' the command is followed by a 16 bit address and the address pointer is loaded with this address. if this is 0 the current address pointer for the memory space is used. Each memory space has its own address pointer.

C Indicates if memory space itself (C=’0') or associated info area for the memory will be accessed (C= ‘1')

M Is the 3 bit memory space specifier 000b through 111b

S Is the transfer element size specifier (00b = 8 bits, 01b = 16 bits 10b = 32 bits and 11b = 64 bits)

I Is the Increment address bit. if this is '1' the address pointer is incremented by the element transfer size (in bytes) after every transfer ('0' is useful for FIFO transfers)

N Is the transfer count in units of the selected size. 1 through 127. A transfer count of 0 is an error.

LBP16 read commands are followed by the 16 bit address (if the A bit is set). LBP16 Write commands are followed by the address (if bit A is set) and the data to be written. LBP16 Addresses are always byte addresses. LBP data and addresses are little endian so must be sent LSB first.

REFERENCE INFORMATION

LBP16

INFO AREA

There are eight possible memory spaces in LBP16. Each memory space has an associated read only info area. The first entry has a cookie to verify correct access. The next two entries in the info area are the MemSizes word and the MemRanges word. Only 16 bit read access is allowed to the info area.

0000	COOKIE = 0X5A0N WHERE N = ADDRESS SPACE 0..7
0002	MEMSIZES
0004	MEMRANGES
0006	ADDRESS POINTER
0008	SPACENAME 0,1
000A	SPACENAME 2,3
000C	SPACENAME 4,5
000E	SPACENAME 6,7

INFO AREA MEMSIZES FORMAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	T	T	T	T	T	T	T	X	X	X	X	A	A	A	A

W Memory space is Writeable

T Is type: 01 = Register, 02 = Memory, 0E = EEPROM, 0F = Flash

A Is access types (bit 0 = 8 bit, bit 1 = 16 bit etc)so for example 0x06 means 16 bit and 32 bit operations allowed

REFERENCE INFORMATION

LBP16

INFO AREA MEMRANGES FORMAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	E	E	E	E	P	P	P	P	P	S	S	S	S	S	S

E Is erase block size

P Is Page size

S Ps address range

Ranges are 2^E, 2^P, 2^S. All sizes and ranges are in bytes. E and P are 0 for non-flash memory

REFERENCE INFORMATION

LBP16

INFO_AREA ACCESS

As discussed above, all memory spaces have an associated information area that describes the memory space. Information area data is all 16 bits and read-only.The hex command examples below are written in LSB first order for convenience. In the hex command examples, the NN is the count/increment field of the LBP16 command and the LLHH is the low and high bytes of the address.

Ispace 0 read with address	NN61LLHH	HostMot2 space
Ispace 0 read	NN21	
Ispace 1 read with address	NN65LLHH	Ethernet chip space
Ispace 1 read	NN25	
Ispace 2 read with address	NN69LLHH	Ethernet EEPROM space
Ispace 2 read	NN29	
Ispace 3 read with address	NN6DLLHH	FPGA flash space
Ispace 3 read	NN2D	
Ispace 6 read with address	NN79LLHH	LBP16 R/W space
Ispace 6 read	NN39	
Ispace 7 read with address	NN7DLLHH	LBP16 R/O space
Ispace 7 read	NN3D	

REFERENCE INFORMATION

LBP16

7I95T SUPPORTED MEMORY SPACES

The 7I95T firmware supports 6 address spaces. These will be described individually with example hexadecimal commands. The hex command examples below are written in LSB first order for convenience. In the hex command examples, the NN is the count/increment field of the LBP16 command and the LLHH is the low and high bytes of the address.

SPACE 0: HOSTMOT2 REGISTERS

This address space is the most important as it gives access to the FPGA I/O. This is a 64K byte address range space with 32 bit R/W access.

Space 0 read with address	NN42LLHH
Space 0 write with address	NNC2LLHH
Space 0 read	NN02
Space 0 write	NN82

REFERENCE INFORMATION

LBP16

SPACE 0: HOSTMOT2 REGISTERS

Example: read first 5 entries in hostmot2 IDROM:

85420004

85	; 85 == NN = 5 | Inc bit (0x80) so address is incremented after each access
42	; Read from space 0 with address included after command
00	; LSB of address (IDROM starts at 0x0400)
04	; MSB of address (IDROM starts at 0x0400)

Example: write 4 GPIO ports starting at 0x1000:

84C20010AAAAAAAABBBBBBBBCCCCCCCCDDDDDDDD

84	; 84 == NN = 4 | Inc bit so address is incremented after each access
C2	; Write to space 0 with address included after command
00	; LSB of address (GPIO starts at 0x1000)
10	; MSB of address (GPIO starts at 0x1000)
AAAAAAAA	; 32 bit data for GPIO port 0 at 0x1000
BBBBBBBB	; 32 bit data for GPIO port 0 at 0x1004
CCCCCCCC	; 32 bit data for GPIO port 0 at 0x1008
DDDDDDDD	; 32 bit data for GPIO port 0 at 0x100C

Note like all LBP16 data, write data is LS byte first

REFERENCE INFORMATION

LBP16

SPACE 1: ETHERNET CHIP ACCESS

Space 1 allows access to the KSZ8851-16 registers for debug purposes. All accesses are 16 bit.

Space 1 read with address	NN45LLHH
Space 1 write with address	NNC5LLHH
Space 1 read	NN05
Space 1 write	NN85

Example: read Ethernet chip CIDER register: 0145C000

01	; = NN = read 1 16 bit value
45	; read space 1 with address included
C0	; LSB of CIDER address
00	; MSB of CIDER address

SPACE 2: ETHERNET EEPROM CHIP ACCESS

This space is used to store the Ethernet MAC address, card name, and EEPROM settable IP address. The Ethernet EEPROM space is accessed as 16 bit data. The first 0x20 bytes are read only and the remaining 0x60 bytes are read/write.

Space 2 read with address	NN49LLHH
Space 2 write with address	NNC9LLHH
Space 2 read	NN09
Space 2 write	NN89

REFERENCE INFORMATION

LBP16

SPACE2: ETHERNET EEPROM CHIP ACCESS

Writes and erases require that the EEPROMWEna be set to 5A02. *Note that EEPROMWEna is cleared at the end of every LPB packet so the write EEPROMWEna command needs to prepended to all EEPROM write and erase packets.* For EEPROM write operations a LBP16 read operation should follow the write(s) for host synchronization.

Example: write EEPROM IP address with 192:168.0.32 (C0:A8:0:20 in hex)

01D91A00025A	Enable EEPROM area writes
82C920002000A8C0	Write 2 words to 0020 : C0A80020 (with inc). Note this must be in the same packet and the EEPROMWEna write

ETHERNET EEPROM LAYOUT

ADDRESS	DATA
0000	Reserved RO
0002	MAC address LS Word RO
0004	MAC address Mid Word RO
0006	MAC address MS Word RO
0008	Reserved RO
000A	Reserved RO
000C	Reserved RO
000E	Unused RO

REFERENCE INFORMATION

LBP16

ETHERNET EEPROM LAYOUT

ADDRESS	DATA
0010	CardNameChar-0,1 RO
0012	CardNameChar-2,3 RO
0014	CardNameChar-4,5 RO
0016	CardNameChar-6,7 RO
0018	CardNameChar-8,9 RO
001A	CardNameChar-10,11 RO
001C	CardNameChar-12,13 RO
001E	CardNameChar-14,15 RO
0020	EEPROM IP address LS word RW
0022	EEPROM IP address MS word RW
0024	EEPROM Netmask LS word RW (V16 and > firmware)
0026	EEPROM Netmask MS word RW (V16 and > firmware)
0028	DEBUG LED Mode (LS bit determines HostMot2 (0) or debug(1)) RW
002A	Reserved RW
002C	Reserved RW
002E	Reserved RW
0030..007E	Unused RW

REFERENCE INFORMATION

LBP16

SPACE 3: FPGA FLASH EEPROM CHIP ACCESS

Space 3 allows access to the FPGAs configuration flash memory. All flash memory access is 32 bit. Flash memory access is different from other memory spaces in that it is done indirectly via a 32 bit address pointer and 32 bit data port.

Space 3 read with address NN4ELLHH

Space 3 write with address NNCELLHHDDDDDDDD

Space 3 read NN0E

Space 3 write NN8E

FLASH MEMORY REGISTERS

Flash memory spaces have only 4 accessible registers:

ADDRESS	DATA	
0000	FL_ADDR	32 bit flash address register
0004	FL_DATA	32 bit flash data register
0008	FL_ID	32 bit read only flash ID register
000C	SEC_ERASE	32 bit write only sector erase register

Unlike other memory spaces, flash memory space is accessed indirectly by writing the address register (FL_ADDR) and then reading or writing the data (FL_DATA). The flash byte address is automatically incremented by 4 each data access.

Note that reads can read all of flash memory with consecutive read operations but write operations can only write a flash page worth of data before the page write must be started. Also unless you are doing partial page writes, page write should always start on a page boundary.

The page write is started by writing the flash address, reading the flash address, reading flash data, reading flash ID or issuing a erase sector command. For host synchronization, a read operation should follow every sector erase or page write.

REFERENCE INFORMATION

LBP16

SPACE 3: FPGA FLASH EEPROM CHIP ACCESS

Example: read 1024 bytes (0100h doublewords) of flash space at address 00123456:

01CE000056341200	Write FL_ADDR (0000) with pointer (0x00123456)
404E0400	Issue read command (FL_DATA = 0004) With count of 0x40 double words (256 bytes). Note do not use LBP16 increment bit! Flash address always autoincremented
400E	Next 0x40 doublewords = 256 bytes
400E	Next 0x40 doublewords = 256 bytes
400E	Next 0x40 doublewords = 256 bytes

Note that this is close to the maximum reads allowed in a single LBP packet (~1450 bytes)

Writes and erases require that the EEPROMWEna be set to 5A03. *Note that EEPROMWEna is cleared at the end of every LPB packet so the write EEPROMWEna command needs to prepended to all flash write and erase packets. The following is written on separate lines for clarity but must all be in one packet for correct operation.*

Example: Write a 256 byte page of flash memory starting at 0xC000:

01D91A00035A	Write EEPROMWEna with 0x5A03
01CE000000C00000	Write flash address
40CE0400	Issue write flash data command with count
12345678	Doubleword 0
ABCD8888	Doubleword 1
...	
FFFFFFFF	Doubleword 63 (= 256 bytes)
014E0000	Read new address to commit write and so some data is returned for host synchronization (so host waits for write to complete)

REFERENCE INFORMATION

LBP16

SPACE 3: FPGA FLASH EEPROM CHIP ACCESS

Example: Erase flash sector 0x00010000:

01D91A00035A	Write EEPROMWEna with 0x5A03
01CE000000000100	Write flash address with 0x 00010000
01CE0C0000000000	Write sector erase command (with dummy 32 bit data = 0)
014E0000	Read flash address for host synchronization (this will echo the address _after_ the sector is erased)

REFERENCE INFORMATION

LBP16

SPACE 4 LBP TIMER/UTILITY AREA

Address space 4 is for read/write access to LBP specific timing registers. All memory space 4 access is 16 bit.

Space 4 read with address	NN51LLHH
Space 4 write with address	NND1LLHHDDDD
Space 4 read	NN11
Space 4 write	NN91DDDD

MEMORY SPACE 4 LAYOUT:

ADDRESS	DATA
0000	uSTimeStampReg
0002	WaituSReg
0004	HM2Timeout
0006	WaitForHM2RefTime
0008	WaitForHM2Timer1
000A	WaitForHM2Timer2
000C	WaitForHM2Timer3
000E	WaitForHM2Timer4
0010..001E	Scratch registers for any use

The uSTimeStamp register reads the free running hardware microsecond timer. It is useful for timing internal 7I95T operations. Writes to the uSTimeStamp register are a no-op. The WaituS register delays processing for the specified number of microseconds when written, (0 to 65535 uS) reads return the last wait time written. The HM2TimeOut register sets the timeout value for all WaitForHM2 times (0 to 65536 uS).

All the WaitForHM2Timer registers wait for the rising edge of the specified timer or reference output when read or written, write data is don't care, and reads return the wait time in uS. The HM2TimeOut register places an upper bound on how long the WaitForHM2 operations will wait. HM2Timeouts set the HM2TImeout error bit in the error register.

REFERENCE INFORMATION

LBP16

SPACE 6 LBP STATUS/CONTROL AREA

Address space 6 is for read/write access to LBP specific control, status, and error registers. All memory space 6 access is 16 bit. The RXUDPCount and TXUDPCount can be used as sequence numbers to verify packet reception and transmission.

Space 6 read with address	NN59LLHH
Space 6 write with address	NND9LLHHDDDD
Space 6 read	NN19
Space 6 write	NN99DDDD

MEMORY SPACE 6 LAYOUT:

ADDRESS	DATA
0000	ErrorReg
0002	LBPParseErrors
0004	LBPMemErrors
0006	LBPWriteErrors
0008	RXPktCount
000A	RXUDPCount
000C	RXBadCount
000E	TXPktCount
00010	TXUDPCount
00012	TXBadCount

REFERENCE INFORMATION

LBP16

MEMORY SPACE 6 LAYOUT:

ADDRESS	DATA	
0014	LEDMode	If LSb is 0, LEDs are "owned" by HostMot2, otherwise LEDs are local debug LEDs
0016	DebugLEDPtr	What variable in space 6 local debug LEDs show (default is RXPktCount).
0018	Scratch	Can be used for sequence numbers
001A	EEPROMWEna	Must be set to 5A0N to enable EEPROM or flash writes or erases (N is memory space of EEPROM or flash) Note that this is cleared at the end of every packet.
001C	LBPReset	Setting this to a non-zero value will do a full reset of the LBP16 firmware. The 7I95T will read ita IP address jumpers and re-assign its IP address. The 7I95T will be unresponsive for as much as ½ of a second after this command.
001E	FPGAICAP	FPGA ICAP-16 register to allow remote FPGA reload and other low level FPGA access.

ERROR REGISTER FORMAT

BIT	ERROR
0	LBPParseError
1	LBPMemError
2	LBPWriteError
3	RXPacketErr
4	TXPacketErr
5	HM2TimeOutError
6..15	Reserved

REFERENCE INFORMATION

LBP16

SPACE 7: LBP READ ONLY AREA

Memory space 7 is used for read only card information. Memory space 7 is accessed as 16 bit data.

Space 7 read with address	NN5DLLHH
Space 7 read	NN1D

MEMORY SPACE 7 LAYOUT:

ADDRESS	DATA	
0000	CardNameChar-0,1	
0002	CardNameChar-2,3	
0004	CardNameChar-4,5	
0006	CardNameChar-6,7	
0008	CardNameChar-8,9	
000A	CardNameChar-10,11	
000C	CardNameChar-12.13	
000E	CardNameChar-14,15	
0010	LBPVersion	
0012	FirmwareVersion	
0014	Option Jumpers	
0016	Reserved	
0018	RecvStartTS	1 uSec timestamps
001A	RecvDoneTS	For performance monitoring
001C	SendStartTS	Send timestamps are
001E	SendDoneTS	from ***previous*** packet

REFERENCE INFORMATION

LBP16

ELBPCOM

ELBPCOM is a very simple demo program in Python (2.x) to allow simple checking of LBP16 host communication to the 7I95T. ELBPCOM accepts hexadecimal LBP16 commands and data and returns hexadecimal results. Note that the timeout value will need to be increased to about 2 seconds to try flash sector erase commands.

```
import socket
s = socket.socket(socket.AF_INET,socket.SOCK_DGRAM,0)
sip  = "192.168.1.121"
sport = 27181
s.settimeout(.2)
while(2 >0):
 sdata = raw_input ('>')
 sdata = sdata.decode('hex')
 s.sendto(sdata,(sip,sport))
 try:
  data,addr = s.recvfrom(1280)
  print ('>'),data.encode('hex')
 except socket.timeout:
  print ('No answer')
```

Sample run:

```
>01420001                       ; read hostmot2 cookie at 0x100
> fecaaa55                      ; 7I95T returns 0x55AACAFE

>82492000                       ; read EEPROM IP address at 0x0020
> 450a5863                      ; 63:58:0A:45 = 99.88.10.69
                                ;(for example)

>01D91A00025A82C920000100a8C0 ; write EEPROM IP address
                                ;(at 0x0020) with
                                ; C0:A8:0:1 = 192.168.0.1
```

REFERENCE INFORMATION

SPECIFICATIONS

	MIN	MAX	NOTES
GENERAL			
HOST SUPPLY VOLTAGE 5V	4.75 VDC	5.25 VDC	
5V CURRENT	----	500 mA	No ext load .
STEP/DIR OUTPUTS			
STEP/DIR OUTPUT HIGH V	4V	----	10 mA source
STEP/DIR OUTPUT LOW V	----	1V	10mA sink
STEP RATE	----	10	MHz
ISOLATED INPUTS			
INPUT RANGE	+-4V	+-36V	
INPUT RESISTANCE	4.7K	5K	
INPUT ISOLATION VOLTAGE	----	100	VDC
MAXIMUM INPUT FREQUENCY	----	5	KHz
ISOLATED OUTPUTS			
OUTPUT SWITCHED VOLTAGE	0V	+36V	
OUTPUT SWITCHED CURRENT	----	2A	
OUTPUT RESISTANCE	----	75	mOhm
OUTPUT ISOLATION VOLTAGE	----	100	VDC
MAXIMUM OUTPUT FREQUENCY	----	5	KHz

REFERENCE INFORMATION

SPECIFICATIONS

		MIN	MAX	NOTES
HIGH SPEED ENCODER INPUTS				
INPUT COMMON MODE RANGE		-7	+12	Volts
INPUT TTL MODE THRESHOLD		1.4	1.8	Volts
DIFFERENTIAL MODE IMPEDANCE		118	122	Ohms
COUNT RATE		----	3 MHz	
RS-422/RS485 INTERFACE				
MAXIMUM DATA RATE		----	5	MBIT/S
INPUT COMMON MODE RANGE		-7	+12	Volts
INPUT TERMINATION RESISTOR		118	122	Ohm
OUTPUT LOW	(24 mA sink)	----	.8	Volts
OUTPUT HIGH	(24 mA source)	VCC-2	----	Volts
EXPANSION I/O				
OUTPUT VOLTAGE LOW		----	.4V	8 mA sink
OUTPUT VOLTAGE HIGH		2.4V	----	8 mA source
ENVIRONMENTAL				
TEMPERATURE -C VERSION		0^oC	70^oC	

REFERENCE INFORMATION

DRAWINGS