# 7I89 MANUAL

**8 channel encoder interface + 1 channel RS-422/RS-485**

V1.0

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# GENERAL

## DESCRIPTION

The 7I89 is a eight channel encoder plus one channel RS-422/RS-485 interface card for Mesa's 25 pin Anything I/O series of FPGA interface cards. The 7I89 is designed for motion control applications. A common usage of the 7I89 would be adding up to 8 incremental encoder channels to a step/dir or Analog servo system. In addition the 7I89 provides one full duplex RS-422 or half duplex RS-485 interface.

Encoder inputs can be TTL or differential on a per input basis. The 7I89 can also supply 5V power to encoders. This encoder power may be switched by the host if desired.

The controller connection is a DB25 connector that matches the pinout of Mesa's 25 pin Anything I/O cards. All buffered I/O is terminated with 3.5 mm pluggable screw terminals (supplied)

# HARDWARE CONFIGURATION

## GENERAL

Hardware setup jumper positions assume that the 7I89 card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side.

## DEFAULT CONFIGURATION

| JUMPER | FUNCTION | DEFAULT SETTING |
|---|---|---|
| W18,W21,W24 | ENCODER 0 MODE | ALL RIGHT = RS-422 |
| W9,W12.W15 | ENCODER 1 MODE | ALL RIGHT = RS-422 |
| W2,W4,W6 | ENCODER 2 MODE | ALL RIGHT = RS-422 |
| W17,W20,W23 | ENCODER 3 MODE | ALL RIGHT = RS-422 |
| W8,W11,W14 | ENCODER 4 MODE | ALL RIGHT = RS-422 |
| W1,W3,W5 | ENCODER 5 MODE | ALL RIGHT = RS-422 |
| W16,W29,W22 | ENCODER 6 MODE | ALL RIGHT = RS-422 |
| W7,W10,W13 | ENCODER 7 MODE | ALL RIGHT = RS-422 |
| W25 | ENCODER 6,7 PWR | UP = ALWAYS ON |
| W26 | ENCODER 3,4,5 PWR | UP = ALWAYS ON |
| W27 | ENCODER 0,1,2 PWR | UP = ALWAYS ON |

## TTL/RS-422 ENCODER SELECTION

Each 7I89 encoder channel has a selectable TTL or RS-422 (differential) encoder input conditioning. Conditioning type is determined by setting groups of 3 jumpers to the right or left position. When the jumpers are in the "LEFT" position, TTL inputs are selected, When the jumpers are in the "RIGHT" position, RS-422 inputs are selected. Note these sets of three jumpers are in physical proximity to the terminal block encoder connections.

## ENCODER POWER OPTION

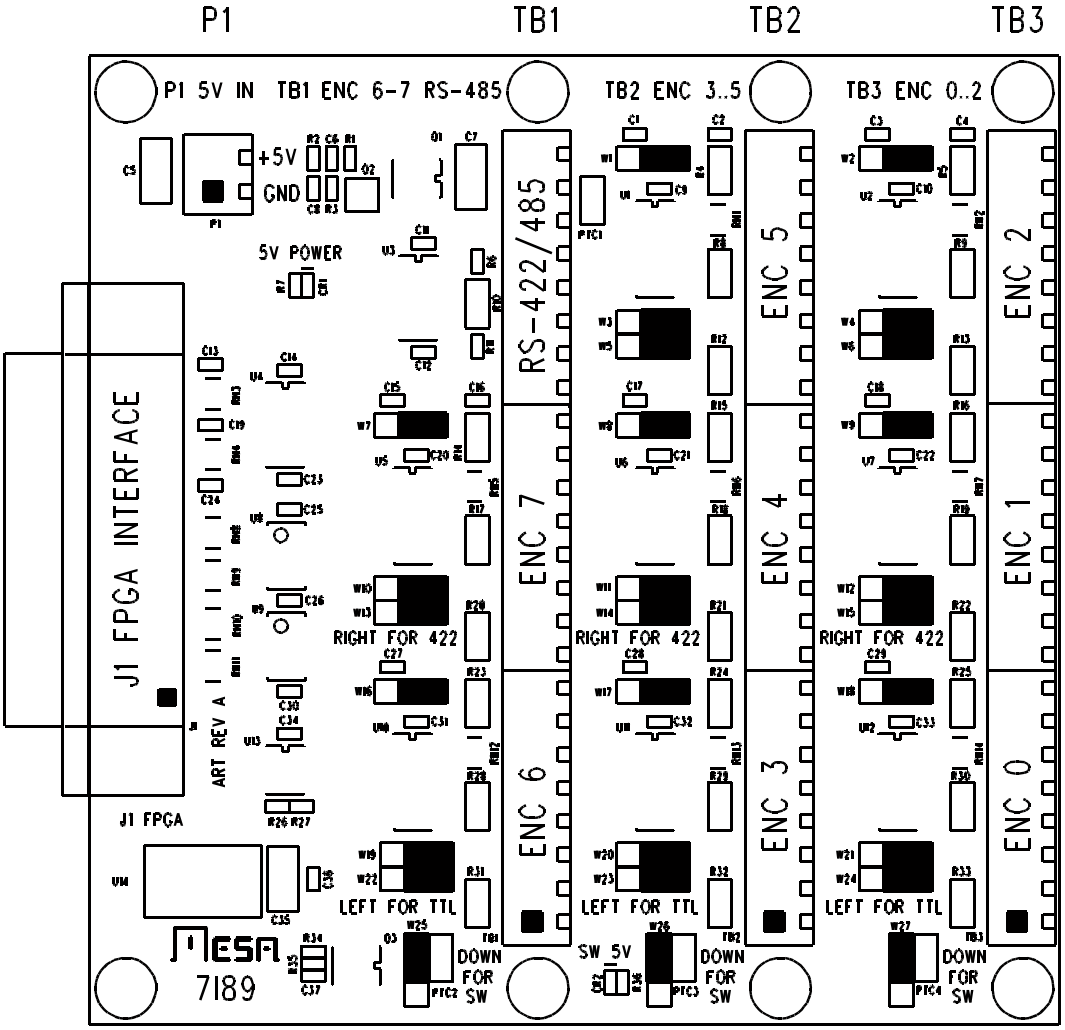
The encoder power on selected encoder channels can be switched under host control. This can be useful for power saving or resetting encoders that transmit absolute encoder position at power on. The option can be selected by setting W25,W26 or W27 into the "UP" position.

## CABLE POWER

The 7I89 gets its 5V power from P1 but requires the host FPGA card to have its cable power option enabled. This is because the 7I89 only enables its local power if the host FPGA card is powered.

# CONNECTORS

## CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONSNote:




Note P1,TB1,TB2,TB3 Pin 1 is marked with a square PAD

# CONNECTORS

## CONTROLLER CONNECTOR

Female 25 pin DB-25F J1 is the host interface connector. This connects to the host interface FPGA card via a IEEE-1284 male-male DB-25 cable.

| DB-25 PIN | FPGA PRIM I/O | FPGA SEC I/O | FUNCTION |
|---|---|---|---|
| 1 | IO0 | IO17 | MUXENCA0 |
| 14 | IO1 | IO18 | MUXENCB0 |
| 2 | IO2 | IO19 | MUXIDX0 |
| 15 | IO3 | IO20 | MUXENCA1 |
| 3 | IO4 | IO21 | MUXENCB1 |
| 16 | IO5 | IO22 | MUXIDX1 |
| 4 | IO6 | IO23 | MUXENCA2 |
| 17 | IO7 | IO24 | MUXENCB2 |
| 5 | IO8 | IO25 | MUXIDX2 |
| 6 | IO9 | IO26 | MUXENCA3 |
| 7 | IO10 | IO27 | MUXENCB3 |
| 8 | IO11 | IO28 | MUXIDX3 |
| 9 | IO12 | IO29 | ENCMUX |
| 10 | IO13 | IO30 | POWOP |
| 11 | IO14 | IO31 | RXD |
| 12 | IO15 | IO32 | TXD |
| 13 | IO16 | IO33 | TXEN |

Note: Pins 18, 19, 20, and 21 are ground. Pins 22, 23, 24 and 25 are 5V

# CONNECTORS

## 5V POWER

2 pin pluggable terminal P1 is used to supply 5V power to logic and the I/O terminals on the 7I89. P1 has the following pinout:

| PIN | FUNCTION |
|---|---|
| 1 | GND |
| 2 | +5V |

# CONNECTORS

## ENCODER CONNECTOR TB3

Connector TB3 is a 3.5MM pluggable screw terminal block with connections for encoder channels 0 through 2:

| TB3 PIN | FUNCTION | DIR |
|---|---|---|
| 1 | QA0 | TO 7I89 |
| 2 | /QA0 | TO 7I89 |
| 3 | GND | FROM 7I89 |
| 4 | QB0 | TO 7I89 |
| 5 | /QB0 | TO 7I89 |
| 6 | +5V | FROM 7I89 |
| 7 | IDX0 | TO 7I89 |
| 8 | /IDX0 | TO 7I89 |
| 9 | QA1 | TO 7I89 |
| 10 | /QA1 | TO 7I89 |
| 11 | GND | FROM 7I89 |
| 12 | QB1 | TO 7I89 |
| 13 | /QB1 | TO 7I89 |
| 14 | +5V | FROM 7I89 |
| 15 | IDX1 | TO 7I89 |
| 16 | /IDX1 | TO 7I89 |
| 17 | QA2 | TO 7I89 |
| 18 | /QA2 | TO 7I89 |
| 19 | GND | FROM 7I89 |
| 20 | QB2 | TO 7I89 |
| 21 | /QB2 | TO 7I89 |
| 22 | +5V | FROM 7I89 |
| 23 | IDX2 | TO 7I89 |
| 24 | /IDX2 | TO 7I89 |

# CONNECTORS

## ENCODER CONNECTOR TB2

Connector TB2 is a 3.5MM pluggable screw terminal block with connections for encoder channels 3 through 5:

| TB2 PIN | FUNCTION | DIR |
|---|---|---|
| 1 | QA3 | TO 7I89 |
| 2 | /QA3 | TO 7I89 |
| 3 | GND | FROM 7I89 |
| 4 | QB3 | TO 7I89 |
| 5 | /QB3 | TO 7I89 |
| 6 | +5V | FROM 7I89 |
| 7 | IDX3 | TO 7I89 |
| 8 | /IDX3 | TO 7I89 |
| 9 | QA4 | TO 7I89 |
| 10 | /QA4 | TO 7I89 |
| 11 | GND | FROM 7I89 |
| 12 | QB4 | TO 7I89 |
| 13 | /QB4 | TO 7I89 |
| 14 | +5V | FROM 7I89 |
| 15 | IDX4 | TO 7I89 |
| 16 | /IDX4 | TO 7I89 |
| 17 | QA5 | TO 7I89 |
| 18 | /QA5 | TO 7I89 |
| 19 | GND | FROM 7I89 |
| 20 | QB5 | TO 7I89 |
| 21 | /QB5 | TO 7I89 |
| 22 | +5V | FROM 7I89 |
| 23 | IDX5 | TO 7I89 |
| 24 | /IDX5 | TO 7I89 |

# CONNECTORS

## ENCODER RS422/485SERIAL CONNECTOR TB1

Connector TB1 is a 3.5MM pluggable screw terminal block with connections for encoder channels 6 and 7 plus the RS-422/RS-485 interface:

| TB1 PIN | FUNCTION | DIR |
|---|---|---|
| 1 | QA6 | TO 7I89 |
| 2 | /QA6 | TO 7I89 |
| 3 | GND | FROM 7I89 |
| 4 | QB6 | TO 7I89 |
| 5 | /QB6 | TO 7I89 |
| 6 | +5V | FROM 7I89 |
| 7 | IDX6 | TO 7I89 |
| 8 | /IDX6 | TO 7I89 |
| 9 | QA7 | TO 7I89 |
| 10 | /QA7 | TO 7I89 |
| 11 | GND | FROM 7I89 |
| 12 | QB7 | TO 7I89 |
| 13 | /QB7 | TO 7I89 |
| 14 | +5V | FROM 7I89 |
| 15 | IDX7 | TO 7I89 |
| 16 | /IDX7 | TO 7I89 |
| 17 | GND | FROM 7I89 |
| 18 | GND | FROM 7I89 |
| 19 | RXD | TO 7I89 |
| 20 | /RXD | TO 7I89 |
| 21 | TXD | FROM 7I89 |
| 22 | /TXD | FROM 7I89 |
| 23 | +5V | FROM 7I89 |
| 24 | +5V | FROM 7I89 |

Note that actual signal functions depend on FPGA configuration.

# OPERATION

## 5V POWER

The 7I89 requires ~300 mA of 5V power for operation. Encoder power and remote serial device power must be added to this figure for total power draw.

Power for the 7I89 logic and encoders is supplied via P1, the 5V power connector. The 5V power to I/O connectors TB1, TB2, and TB3 each pass through a 2.0 A PTC device before being routed to the I/O terminals. This limits the I/O power supplied by TB1, TB2, and TB3 to ~1.2 A each in 0 to 70C ambients. 5V power status is indicated by yellow LED CR1.

## ENCODER INPUT CIRCUIT

The 7I89 input circuit is different depending on whether TTL or RS-422 (differential) encoder types have been selected. In TTL mode the input circuit on the encoder QA, QB, and IDX inputs drive one input of the RS-422 differential receiver, and the other receiver input is terminated to a 1.65V (TTL threshold) reference voltage. In RS-422 mode, the input consists of a 120 Ohm termination resistor and a 26LS32 RS-422 differential receiver.

When TTL encoders are used, they connect to the 'True' input of the differential pair, for example a TTL encoder for channel 2 would connect to QA2, QB2 and IDX2, while the /QA2, /QB2, and /IDX2 terminals would be left open.

Fine print: normally the input mode jumpers would always be moved as a sets of three to select TTL or RS-422 mode for individual encoders, however it is possible to select TTL or RS-422 mode for each encoder signal, for example if a encoder had a differential A, B but TTL index, the input circuit can accommodate this. The three input mode select jumpers are in bottom to top order: QA, QB, IDX.

## ENCODER POWER OPTION

The 7I89 can enable encoder 5V power via a host control pin. This can be used for encoders that can be reset at power on and transmit absolute encoder data or to save power when idle. The encoders on each terminal block can be set for always on or switchable 5V power. Power to switchable 5V is controlled by the /POWOP pin on the FPGA interface. /POWOP is active low (low for on). Switched power state is indicated by yellow LED CR2.

# OPERATION

## MAXIMUM ENCODER COUNT RATE

The 7I89 uses multiplexed encoder signals to save interface pins. The multiplexing rate will determine the maximum encoder count rate. Default multiplexing rate with HostMot2 firmware is ClockLow / 8,or approximately 4 or 6 MHz, giving a resolvable count rate of 2 to 3 MHz. Multiplexing rate can be increased if desired but high multiplex rates will require short cables between the FPGA controller card and the 7I89 due to signal integrity and time-of-flight considerations. Maximum practical multiplex rate is approximately 12 MHz (and 6 MHz count rates). Encoder count rate is further limited by HostMot2s input filtering to ~5 to ~8 million counts per second (encoder filtering off) and ~1 to ~1.6 million counts per second (encoder filtering on).

## INTERFACING WITH MESA SSERIAL DEVICES

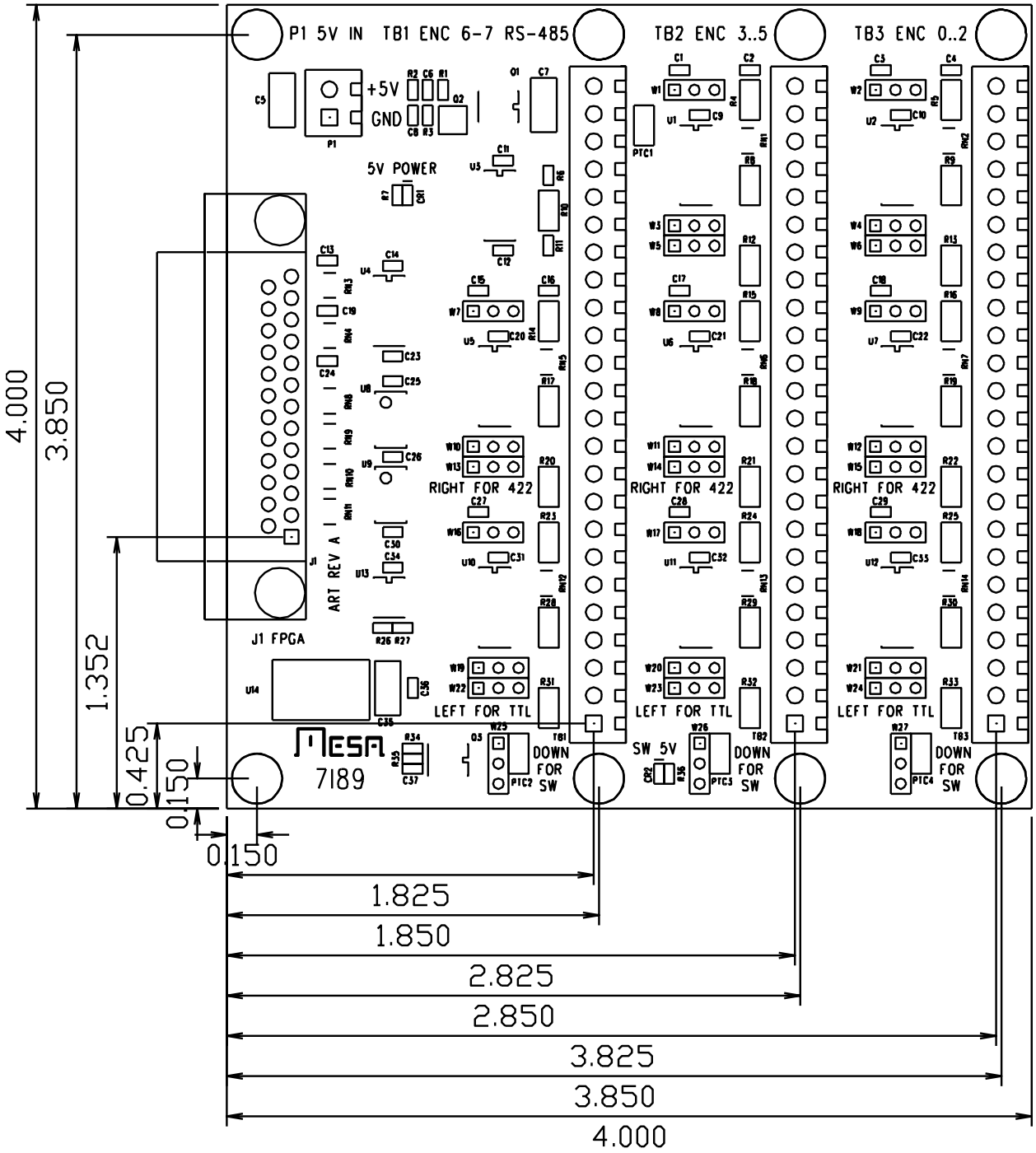
The 7I89s singe differential serial interface is intended to be a general purpose RS-422/RS-485 use but can easily interface to MESA's SSerial I/O devices that use RS-422 communication and RJ45/CAT5 cable for the interface.. The easiest way to make a cable for interfacing the 7I89 to these devices is to take a standard CAT5 or CAT6 cable, cut it in half, and wire the individual wires to the 7I89 screw terminals. The following chart gives the CAT5 to 7I89 screw terminal connections (EIA/TIA 568B colors shown):

| 7I89 TB3 | 7I89 SIGNAL | DIRECTION | CAT5 PIN | CAT5 568B COLOR |
|---|---|---|---|---|
| 17 | GND | FROM 7I89 | 4 | BLUE |
| 18 | GND | FROM 7I89 | 5 | BLUE / WHITE |
| 19 | RX+ | TO 7I89 | 6 | GREEN |
| 20 | RX- | TO 7I89 | 3 | GREEN / WHITE |
| 21 | TX+ | FROM 7I89 | 2 | ORANGE |
| 22 | TX- | FROM 7I89 | 1 | ORANGE / WHITE |
| 23 | +5V | FROM 7I89 | 7 | BROWN / WHITE |
| 24 | +5V | FROM 7I89 | 8 | BROWN |

# SPECIFICATIONS

| | MIN | MAX | UNITS |
|---|---|---|---|
| 5V POWER SUPPLY | 4.75 | 5.25 | VDC |
| 5V POWER CONSUMPTION | --- | 300 | mA |
| (all outputs loaded with 130 ohm terminations) | | | |
| (no external encoder or serial 5V load) | | | |
| 5V CURRENT TO EACH I/O CONNECTOR | --- | 1.2 | A |
| MAXIMUM DATA RATE | --- | 10 | MBIT/S |
| RS-422 INPUT COMMON MODE RANGE | -7 | +12 | Volts |
| RS-422 TERMINATION RESISTANCE | 118 | 122 | Ohm |
| RS-422 OUTPUT LOW | — | .8 | Volts |
| (24 mA sink current) | | | |
| RS-422 OUTPUT HIGH | VCC-2.5 | — | Volts |
| (24 mA source current) | | | |
| ENC INPUT COMMON MODE RANGE | -7 | +12 | Volts |
| ENC INPUT TTL MODE THRESHOLD | 1.4 | 1.8 | Volts |
| OPERATING TEMP. | 0 | +70 | $^{o}$C |
| OPERATING TEMP. (-I version) | -40 | +85 | $^{o}$C |
| OPERATION HUMIDITY | 0 | 95% | NON-COND |

# DRAWINGS


P1 5V IN
TB1 ENC 6-7 RS-485
TB2 ENC 3..5
TB3 ENC 0..2
+5V
GND
5V POWER
RIGHT FOR 422
LEFT FOR TTL
DOWN FOR SW
SW 5V
J1 FPGA
ART REV A
7I89
4.000
3.850
1.352
0.425
0.150
0.150
1.825
1.850
2.825
2.850
3.825
3.850
4.000