7188 MANUAL

16 differential output interface

V1.0

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GENERAL

DESCRIPTION

The 7I88 is a 16 channel differential driver that can provide up to 8 differential Step/Dir or 8 PWM/Dir output channels or other 5V differential output options. The last channel pair can be be used as a RS-485 interface if desired. All differential outputs have a full 5V swing and can be used single ended if required. 5V and GND connections are provided for all channels. The controller connection is a DB25 connector that matches the pinout of Mesa's 25 pin Anything I/O cards. All buffered I/O is terminated with 3.5 mm pluggable screw terminals (supplied)

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I85S card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side.

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W1	CABLE/AUX 5V POWER	UP = CABLE 5V POWER
W2,W3,W4,W5	RS-485 ENABLE	ALL UP = RS-485 DISABLED

RS-485 ENABLE

The last Step/Dir channel (D14 and D15) can be used as a RS-422/RS-485 serial link compatible with Mesa SSerial devices. To enable this option, W2,W3,W4,W5 must all be moved to the "DOWN" position.

CABLE POWER

The 7I88 can get its logic power from the host FPGA card or from P1. W1 determines if the 7I88 gets its 5V logic power from the host FPGA card or P1.

If W3 is in the 'UP' position, host FPGA power is used and the host FPGA card must be jumpered to supply 5V to the daughtercard.

If W3 is in the 'DOWN' position, 5V power must be supplied to the 7I85S via P1 and the 7I88 grounds the 4 DB25 signals used for host 5V power. In this case the FPGA card must be jumpered so that it does **not** supply power to the daughtercard.

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



Note: TB1,TB2,TB3 Pin 1 is marked with square on board

CONTROLLER CONNECTOR

Female 25 pin DB-25F P1 is the host interface connector. This connects to the host interface FPGA card via a IEEE-1284 male-male DB-25 cable.

DB-25 PIN	FPGA PRIM I/O	FPGA SEC I/O	FUNCTION
1	IO0	IO17	D0/Step0
14	IO1	IO18	D1/Dir0
2	IO2	IO19	D2/Step1
15	IO3	IO20	D3/Dir1
3	IO4	IO21	D4/Step2
16	IO5	IO22	D5/Dir2
4	IO6	IO23	D6/Step3
17	107	IO24	D7/Dir3
5	IO8	IO25	D8/Step4
6	IO9	IO26	D9/Dir4
7	IO10	IO27	D10/Step5
8	IO11	IO28	D11/Dir5
9	IO12	IO29	D12/Step6
10	IO13	IO30	D13/Dir6
11	IO14	IO31	D14/Step7/TXEN
12	IO15	IO32	D15/Dir7TXDATA
13	IO16	IO33	RXDATA

Pins 18, 19, 20, and 21 are ground. Pins 22, 23, 24 and 25 are either ground or 5V depending on jumper W1 (ground if W1 "DOWN", 5V if W1 "UP").

5V POWER

2 pin pluggable terminal P1 can be used to supply 5V power to the I/O terminals on the7I85S. This is suggested for applications where the encoders or remote serial cards draw more current than can be supplied via the host interface cable. P1 has the following pinout:

PIN FUNCTION

- 1 GND
- 2 +5V

DIFFERENTIAL OUTPUT CONNECTOR TB2

Connector TB2 is a 3.5MM pluggable screw terminal block with differential output channels 0 through 7.

TB2 PIN	FUNCTION
1	GND
2	D0/STEP0-
3	D0/STEP0+
4	D1/DIR0-
5	D1/DIR0+
6	+5V
7	GND
8	D2/STEP1-
9	D2/STEP1+
10	D3/DIR1-
11	D3/DIR1+
12	+5V
13	GND
14	D4/STEP2-
15	D4/STEP2+
16	D5/DIR2-
17	D5/DIR2+
18	+5V
19	GND
20	D6/STEP3-
21	D6/STEP3+
22	D7/DIR3-
23	D7/DIR3+
24	+5V

Note that actual signal functions depend on FPGA configuration.

DIFFERENTIAL OUTPUT CONNECTOR TB3

Connector TB3 is a 3.5MM pluggable screw terminal block with differential output channels 8 through 15.

TB2 PIN	FUNCTION
1	GND
2	D8/STEP4-
3	D8/STEP4+
4	D9/DIR4-
5	D9/DIR4+
6	+5V
7	GND
8	D10/STEP5-
9	D10/STEP5+
10	D11/DIR5-
11	D11/DIR5+
12	+5V
13	GND
14	D12/STEP6-
15	D12/STEP6+
16	D13/DIR6-
17	D13/DIR6+
18	+5V
19	GND
20	D14/STEP7-
21	D14/STEP7+
22	D15/DIR7-
23	D15/DIR7+
24	+5V

Note that actual signal functions depend on FPGA configuration.

OPERATION

5V POWER

The 7I88 requires ~50 mA of 5V power for operation. This power will increase based on the number of terminated differential outputs used, up to a maximum of ~700 mA of local logic power if all differential outputs are terminated with 100 Ohms.

Power for the 7I88 logic is normally supplied from the host interface but can also be supplied via P1, the 5V power connector.

The 5V power to I/O connectors TB2 and TB3 each pass through a 1.1A PTC device before being routed to the I/O terminals. This limits the 5V power supplied by TB2, and TB3 to \sim 640 mA each in 0 to 70C ambients.

OPERATION

INTERFACING WITH MESA SERIAL DEVICES

The 7I88 serial port is intended to be a general purpose RS-485/RS-422 serial interface but can easily interface to MESA's serial I/O devices that use RS-422 communication and RJ45/CAT5 cable for the serial interface. These devices include the 7I64 Isolated I/O interface, the 8I20 3 phase drive, the 7I66 isolated I/O interface, the 7I69 TTL I/O interface and the 7I73 pendant interface. The easiest way to make a cable for interfacing the 7I88 to these devices is to take a standard CAT5 or CAT6 cable, cut it in half, and wire the individual wires to the 7I88 screw terminals. The following chart gives the CAT5 to 7I85 screw terminal connections (EIA/TIA 568B colors shown):

TB3 PIN	SIGNAL	DIRECTION	CAT5 PIN	CAT5 568B COLOR
19	GND	FROM 7188	4,5	BLUE, BLUE / WHITE
20	RX+	TO 7188	6	GREEN
21	RX-	TO 7188	3	GREEN / WHITE
22	TX+	FROM 7188	2	ORANGE
23	TX-	FROM 7188	1	ORANGE / WHITE
24	+5V	FROM 7188	7,8	BROWN/WHITE,BROWN

Note: The 6 pin terminal block requires the +5V (brown and brown/white) and ground (blue and blue/white) pairs to be terminated in single screw terminal positions.

For 2 wire RS-485 applications, TX+ must be connected to RX+ and TX- must be connected to RX-.

INTERFACING TO DRIVES

The 7I88 differential outputs have full 5V swing and can interface to drives with differential or single ended inputs. For drives that accept differential inputs, differential wiring should be used, with twisted pairs connecting the 7I88s + and - outputs to the corresponding drive pins. In this case the ground connection should connect to the drive ground and cable shield and not be connected at the 7I88.

For drives that only have single ended inputs, +5V is provided for drives with a common + (common anode optocouplers etc), and a GND connection is provided for drives with a common - (common cathode optocouplers etc). When using a common +5V normally the DN- outputs are used and the DN+ outputs are left open. When using a common GND, normally the DN+ signals are used and the DN- outputs left open.

OPERATION

DIFFERENTIAL OUTPUT DRIVE

The 7I88 outputs are designed to drive singly terminated RS-422 lines or remote opto-isolator diodes. Maximum output drive is 50 mA. The 7I88 outputs can be used individually for interfacing single ended loads.

STARTUP OUTPUT POLARITY AND STATE

When 7188 outputs are used for drive enables or other safety related controls its very important that the startup state disables the external equipment.

The differential outputs are polarized such that the DN- pins are inverted from the FPGA pins and the DN+ pins are non inverting. Since the FPGA cards outputs are high at startup, the DN- pins will be low at startup (and therefore suitable for active high enables). The DN+ pins will be high at startup (and suitable for active low enables).

SPECIFICATIONS

	MIN	MAX	UNITS		
5V POWER SUPPLY	4.75	5.25	VDC		
5V POWER CONSUMPTION		750	mA		
(All differential outputs loaded with 100 Ohm terminations)					
5V CURRENT TO EACH I/O CONNECTOR		640	mA		
MAXIMUM DATA OUTPUT RATE		32	MBIT/S		
RS-422 OUTPUT LOW	_	0.4	Volts		
(24 mA sink current)					
RS-422 OUTPUT HIGH	VCC- 0.4V	_	Volts		
(24 mA source current)					
SERIAL PORT MAXIMUM DATA RATE	_	5	Mbps		
OPERATING TEMP.	0	+70	°C		

DRAWINGS

