7I75 MANUAL

FPGA I/O PROTECTOR / BREAKOUT

V1.3

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GENERAL

DESCRIPTION

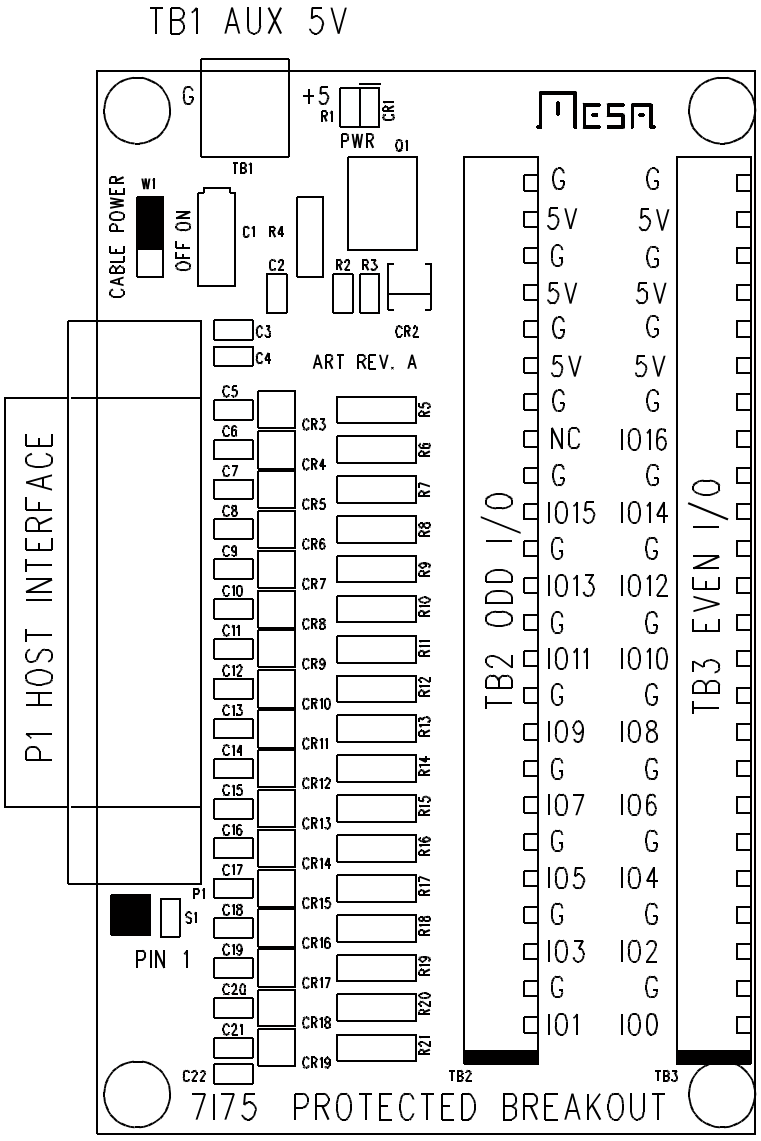
The 7I75 is a breakout card for Mesa's 25 pin I/O FPGA cards. It is available with In addition to providing a breakout function, the 7I75 protects the FPGA card from excessive input voltages and ESD. The 7I75 protects FPGA I/O from accidental contact from external voltages of +12 and -5V with built in diode clamps and 50 Ohm current limit resistors in series with all I/O pins. The 7I75 limits I/O pin bandwidth to approximately 10 MHz. Phoenix compatible 3.5 mm pluggable screw terminals are supplied with the 7I75

OPTION JUMPERS

The 7I75 has a single option jumper: W1. W1 determines if the 7I75 card gets its power from host connector (P1). When W1 is in the up position (default), the 7I75 cards gets its power from the FPGA host interface card. When W1 is in the down position, The 7I75 must be supplied with external 5V power via TB1.

CONNECTORS

7I75 CONNECTOR LOCATIONS



CONNECTORS

CONTROLLER CONNECTOR

Female 25 pin DB-25F P1 is the host interface connector. This connects to the host interface FPGA card via a IEEE-1284 male-male DB-25 cable.

DB-25 PIN	FPGA PRIMARY I/O	FPGA SECONDARY I/O
1	IO0	IO17
14	IO1	IO18
2	IO2	IO19
15	IO3	IO20
3	IO4	IO21
16	IO5	IO22
4	IO6	IO23
17	IO7	IO24
5	IO8	IO25
6	IO9	IO26
7	IO10	IO27
8	IO11	IO28
9	IO12	IO29
10	IO13	IO30
11	IO14	IO31
12	IO15	IO32
13	IO16	IO33

Pins 18, 19, 20, and 21 are ground. Pins 22, 23, 24 and 25 are either ground or 5V depending on jumper W1 (ground if W1 "DOWN", 5V if W1 "UP")

CONNECTORS

AUX 5V POWER

Two pin terminal block TB1 can be used to supply 5V power to the 7I75 if the controller cable is too long and voltage drop too high. TB1 has the following pinout:

PIN	FUNCTION
1	5V (Square pad)
2	GND

PROTECTED I/O CONNECTORS

The 7I75 uses 3.5 mm pluggable screw terminal blocks TB1 and TB2 for protected I/O. TB1 pinout is as follows:

TB1: EVEN PROTECTED I/O PINS

PIN	FUNCTION	PIN	FUNCTION
1	PROTECTED I/O0	2	GND
3	PROTECTED I/O2	4	GND
5	PROTECTED I/O4	6	GND
7	PROTECTED I/O6	8	GND
9	PROTECTED I/O8	10	GND
11	PROTECTED I/O10	12	GND
13	PROTECTED I/O12	14	GND
15	PROTECTED I/O14	16	GND
17	PROTECTED I/O16	18	GND
19	5V	20	GND
21	5V	22	GND
23	5V	24	GND

CONNECTORS

PROTECTED I/O CONNECTORS

TB2: ODD PROTECTED I/O PINS

PIN	FUNCTION	PIN	FUNCTION
1	PROTECTED I/O1	2	GND
3	PROTECTED I/O3	4	GND
5	PROTECTED I/O5	6	GND
7	PROTECTED I/O7	8	GND
9	PROTECTED I/O9	10	GND
11	PROTECTED I/O11	12	GND
13	PROTECTED I/O13	14	GND
15	PROTECTED I/O15	16	GND
17	NC	18	GND
19	5V	20	GND
21	5V	22	GND
23	5V	24	GND

OPERATION

PINOUT

The 7I75 is intended to operate with 25 pin FPGA I/O cards like the Mesa 5I25 and Mesa 6I25**.**

The 7I75 accepts 3.3V or 5V signals but will not protect 3.3V only cards from 5V inputs, as its input clamp voltage is 4.6V

DRIVE STRENGTH

The 7I75 places 50 Ohm resistors in series with each I/O pin. These resistors will limit the output drive capabilities of the attached FPGA card. When the 7I75 is used and FPGA outputs are programmed for 24 mA drive, no more than 8 mA loads should be driven if TTL output levels are to be maintained.

INPUT CLAMP

The 7I75 uses diode clamps to protect the attached FPGA card from excessive input voltage. Nominal upper clamp voltage is 4.6V and nominal lower clamp voltage is -0.7V. Maximum positive input voltage is +12V and maximum negative input voltage is -5V. Note: the 7I75 is designed to protect FPGA cards from transient and accidental connection to voltages outside of their safe I/O range. It is not designed as a input clamp for continuous overvoltages.

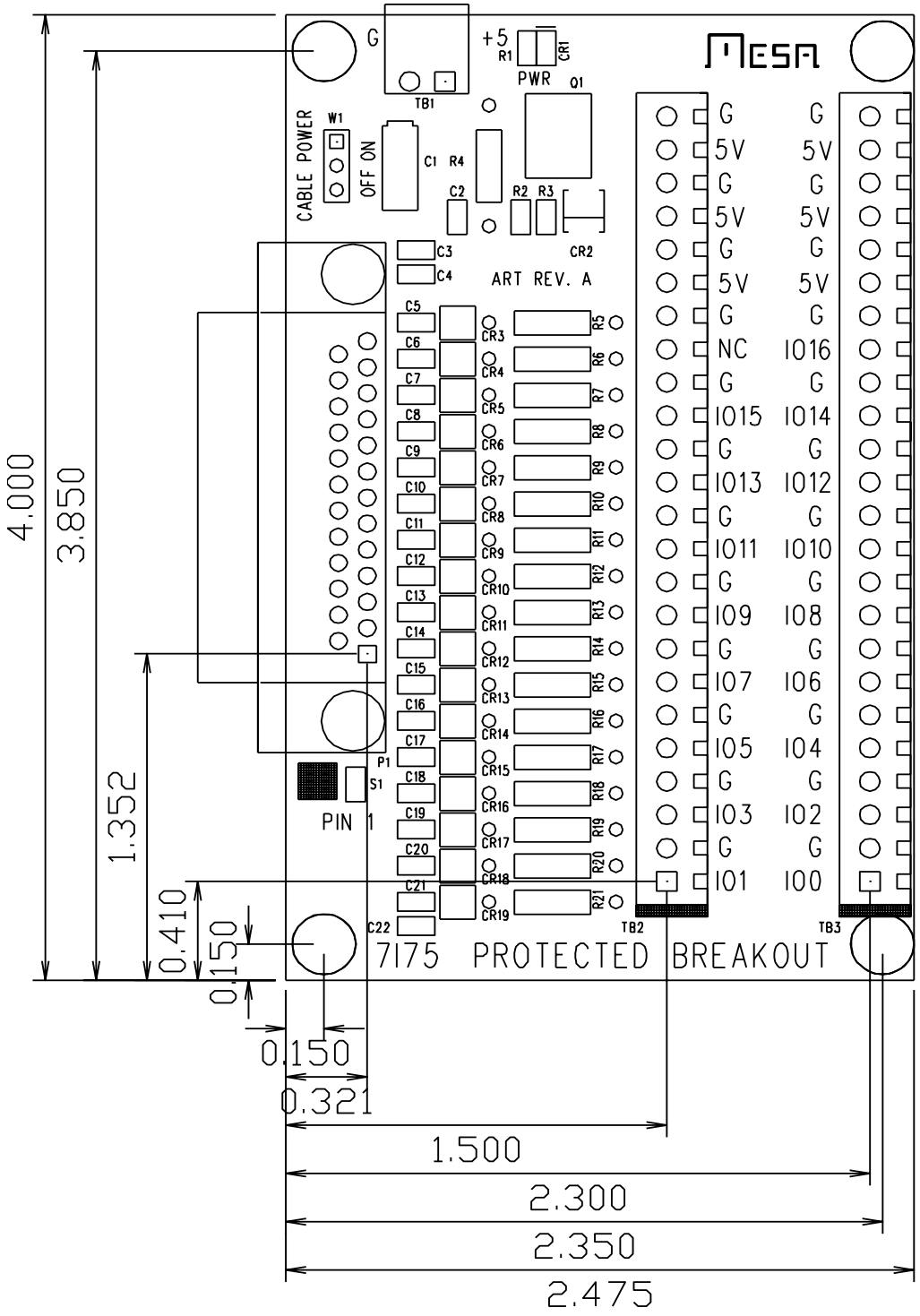
BANDWIDTH

The 7I75s 50 Ohm series resistors and parallel 220 pF capacitors limit the protected signal bandwidth to approximately 10 MHz.

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.5V	5.5V	VDC
5V POWER CONSUMPTION	---	50	mA
INPUT RANGE	-5	+12V	VDC
MAXIMUM NUMBER OF INPUTS	----	4	INPUTS
WITH SIMULTANEOUS 12V OVERLOAD			
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND

DRAWINGS


MESA
7I75 PROTECTED BREAKOUT
ART REV. A
CABLE POWER
OFF ON
PWR
PIN 1
TB1
TB2
TB3
P1
S1
W1
Q1
CR1
CR2
4.000
3.850
1.352
0.410
0.150
0.150
0.321
1.500
2.300
2.350
2.475