

# **7168 3X2X MOTHERBOARD MANUAL**

Preliminary version 1.2

This page intentionally not blank

—

# Table of Contents

GENERAL .....	1
DESCRIPTION .....	1
HARDWARE CONFIGURATION .....	2
GENERAL .....	2
EEPROM DISABLE .....	2
FORCE-ON .....	3
CONNECTOR POWER .....	3
BUS SWITCH MODE .....	3
AUTCONFIG .....	4
VIOSELECT .....	4
7168 / MODULE PIN CORRESPONDENCE	
CONNECTORS .....	5
CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS .....	5
I/O CONNECTOR PIN-OUT .....	6
DIFFERENTIAL PAIRS .....	12
JTAG PINOUT .....	12
PCIE PINOUT .....	12
OPERATION .....	13
LEDS .....	13
I/O LEVELS .....	13
STARTUP I/O VOLTAGE .....	13
POWER SUPPLY .....	13
POWER SUPPLY ENABLE .....	13
REFERENCE INFORMATION .....	14
SPECIFICATIONS .....	14

# GENERAL

## DESCRIPTION

The MESA 7I68 is a motherboard for Mesas' 3X2X series of FPGA daughtercards. The 7I68 breaks out the high density daughterboard I/O connections into six 50 pin .1" headers with standard AnythingIO pinouts. The 7I68 also provides up to 3A of 3.3V power for the daughtercard via an on card switching regulator. Bus switches are provided on all 144 I/O pins to allow interfacing with 5V I/O.

# HARDWARE CONFIGURATION

## GENERAL

Hardware setup jumper positions assume that the 7I68 card is oriented in an upright position, that is, with the PCI connector facing the user, and the white PCB markings right side up.

## DEFAULT SETUP

EEPROM ENABLED	W9 UP
AUTOCONFIG DISABLED	W8 DOWN
RIGHT AND LEFT VIO = 3.3V	W6,W7,W10,W11 UP
CONNECTOR POWER = 5V (ALL)	W12,W13,W14,W2,W3,W4 LEFT
BUS SWITCH MODE = 3.3V	W1,W15 RIGHT
FORCE_ON DISABLED	W5 DOWN

These default jumper positions are shown in the default jumper position picture on page 5.

## EEPROM ENABLE

On the 3X20 module, the PCI9056 part of the PEX8311 PCIE-Local bus bridge chip is configured at power up via a serial EEPROM. If the EEPROM is somehow mis-programmed or corrupted, it can be impossible to re-write the EEPROM from the PCI bus. To avoid this problem, The EEPROM can be temporarily disabled. W9 controls the EEPROM enable function, When W9 is in the up position (default) the EEPROM is enabled. When W9 is in the down position, the EEPROM is disabled. To fix a broken EEPROM setup, you must power up the 7I68 and module card with the EEPROM disabled, Enable the EEPROM, and re-write the EEPROM.

## FORCE\_ON

Normally, the 7I68 powers up when the PCIE cable CPWRON signal is asserted. For standalone applications or applications when the FPGA card must continue to operate when the host is powered down, the FORCE\_ON option is provided. When the FORCE\_ON jumper (W5) is in the down position, the 7I68 power supply is switched via CPWRON. When W5 is in the up position, the 7I68 will be powered regardless of the state of CPWRON.

# HARDWARE CONFIGURATION

## CONNECTOR POWER

The power connection on the I/O connectors pin 49 can supply either 3.3V or 5V power. Supplied power should be limited to 400 mA per connector.

When the following jumpers are in the left position, 5V power is supplied to pin 49 of the associated connector. When the jumper is in the right position, 3.3V power is supplied to to pin 49 of the associated connector.

W12 selects the voltage supplied to P4. (I/O connector for bits 0..23)

W13 selects the voltage supplied to P5. (I/O connector for bits 24..47)

W14 selects the voltage supplied to P6. (I/O connector for bits 48..71)

W4 selects the voltage supplied to P9. (I/O connector for bits 72..95)

W3 selects the voltage supplied to P8. (I/O connector for bits 96..119)

W2 selects the voltage supplied to P7. (I/O connector for bits 120..143)

## BUS SWITCH MODE

The 7I68 uses bus switch devices in series with all I/O pins. These devices allow the 3X2X inputs to be 5V tolerant and allow the I/O pins to be pulled up to 5V. The bus switch input protection function works by disconnecting the FPGA from the IO pins when the IO pin voltage rises above a preset threshold. This threshold determines the bus switch operational mode and is selectable for the three left hand I/O connectors and the three right hand I/O connectors separately. We refer to the modes as 5V mode and 3.3V mode.

When in 5V mode, the inputs and tri-stated outputs may be pulled up to 5V. This allows driving 5V referred loads such as I/O module racks. The disadvantage of 5V mode is that the output impedance is higher in the high output state (when the FPGA pins are at 3.3V) as the bus switch is off when the FPGA pin is at 3.3V. When 3.3V mode is selected, the bus switch is always fully on unless input voltages >4V are applied, at which point the bus switch disconnects the FPGA from the I/O pin. 3.3V mode is suggested for general use.

When the bus switch mode jumper is in the left position, 5V mode is selected, when right, 3.3V bus switch mode is selected.

W1 Sets bus switch mode for P4,P5,P6, = IO 0..71

W15 Sets bus switch mode for P9,P8,P6 = IO 72..143

# HARDWARE CONFIGURATION

## AUTOCONFIG

The 3X2X modules can be configured via the PCIE bus or from their local EEPROM. W8 determines the configuration mode. When W8 is in the down position, the 3X2X module will start up unconfigured and must be configured from the PCIE host. When W8 is in the up position, the 3X2X module will be configured via its on card EEPROM.

## I/O VOLTAGE SELECT

The 3X2X modules have three separate I/O power supplies, with each I/O bank having 48 I/O signals. One bank has a fixed I/O voltage of 3.3V, while the other 2 banks have selectable I/O voltages. Two voltage select pins are provided for each of the banks with selectable voltages :

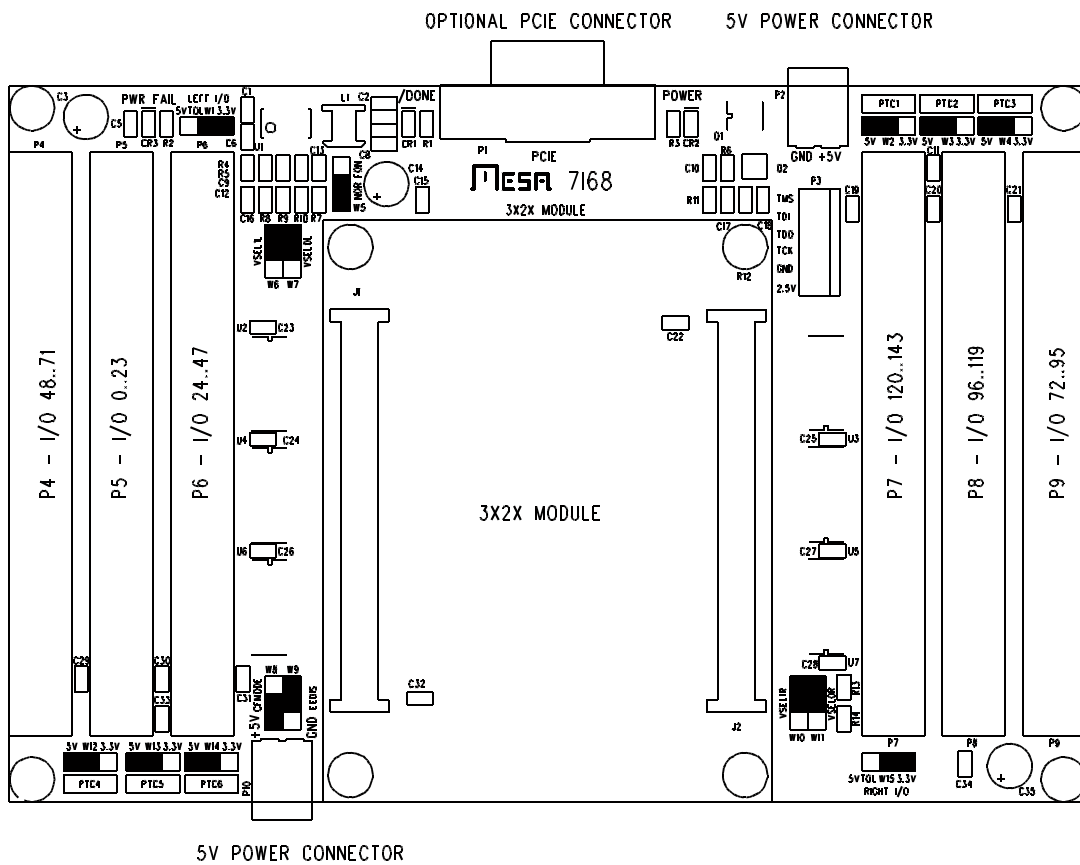
<b>W6</b>	<b>W7</b>	<b>LEFT VIO</b>
DOWN	DOWN	1.5V
DOWN	UP	1.8V
UP	DOWN	2.5V
UP	UP	3.3V
<b>W10</b>	<b>W11</b>	<b>RIGHT VIO</b>
DOWN	DOWN	1.5V
DOWN	UP	1.8V
UP	DOWN	2.5V
UP	UP	3.3V

## 7I68 / MODULE PIN CORRESPONDENCE

In order to simplify the differential pair routing on the 7I68, the 7I68s' I/O pin names have been changed from the 3X2X pin names. This affects the pins with selectable I/O voltages. The 7I68s' I/O connectors all end up with 16 I/O pins with selectable VIO and 8 pins with a fixed 3.3VIO on each connector. Note that FPGA configuration used with a 7I68 needs to use the proper ucf file with 7I68 pinouts. These ucf files should have 7I68 or 6I68 in their name.

# CONNECTORS

## CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



# CONNECTORS

## I/O CONNECTORS

P4, P5, P6,P9,P8, and P7 are the 7i68s I/O connectors. These are 50 pin box headers that mate with standard 50 conductor female IDC connectors. Suggested mating connector is AMP PN 1-1658621-0.. P4 pinout with 3X20 is as follows:

<b>7I68 I/O</b>	<b>3X20 I/O</b>	<b>FPGA BALL</b>	<b>P4 PIN</b>	<b>VIO GROUP</b>
IO48	IO0	B11	1	LEFT VIO
IO49	IO1	A11	3	LEFT VIO
IO50	IO6	B9	5	LEFT VIO
IO51	IO7	A9	7	LEFT VIO
IO52	IO12	B7	9	LEFT VIO
IO53	IO13	A7	11	LEFT VIO
IO54	IO18	E6	13	LEFT VIO
IO55	IO19	D6	15	LEFT VIO
IO56	IO24	D1	17	LEFT VIO
IO57	IO25	C1	19	LEFT VIO
IO58	IO30	E1	21	LEFT VIO
IO59	IO31	E2	23	LEFT VIO
IO60	IO36	G1	25	LEFT VIO
IO61	IO37	G2	27	LEFT VIO
IO62	IO42	J4	29	LEFT VIO
IO63	IO43	H4	31	LEFT VIO
IO64	IO48	M2	33	FIXED 3.3VIO
IO65	IO49	M1	35	FIXED 3.3VIO
IO66	IO54	N4	37	FIXED 3.3VIO
IO67	IO55	N3	39	FIXED 3.3VIO
IO68	IO60	T3	41	FIXED 3.3VIO
IO69	IO61	R4	43	FIXED 3.3VIO
IO70	IO66	V2	45	FIXED 3.3VIO
IO71	IO67	V1	47	FIXED 3.3VIO

# CONNECTORS

## I/O CONNECTORS

P5 pinout with 3X20 is as follows:

<b>7I68 I/O</b>	<b>3X20 I/O</b>	<b>FPGA BALL</b>	<b>P5 PIN</b>	<b>VIO GROUP</b>
IO0	IO2	D11	1	LEFT VIO
IO1	IO3	C11	3	LEFT VIO
IO2	IO8	B8	5	LEFT VIO
IO3	IO9	A8	7	LEFT VIO
IO4	IO14	E7	9	LEFT VIO
IO5	IO15	D7	11	LEFT VIO
IO6	IO20	D5	13	LEFT VIO
IO7	IO21	C5	15	LEFT VIO
IO8	IO26	D3	17	LEFT VIO
IO9	IO27	D2	19	LEFT VIO
IO10	IO32	F4	21	LEFT VIO
IO11	IO33	E3	23	LEFT VIO
IO12	IO38	G3	25	LEFT VIO
IO13	IO39	G4	27	LEFT VIO
IO14	IO44	J1	29	LEFT VIO
IO15	IO45	J2	31	LEFT VIO
IO16	IO50	M4	33	FIXED 3.3VIO
IO17	IO51	M3	35	FIXED 3.3VIO
IO18	IO56	P2	37	FIXED 3.3VIO
IO19	IO57	P1	39	FIXED 3.3VIO
IO20	IO62	T2	41	FIXED 3.3VIO
IO21	IO63	T1	43	FIXED 3.3VIO
IO22	IO68	V4	45	FIXED 3.3VIO
IO23	IO69	V3	47	FIXED 3.3VIO

# CONNECTORS

## I/O CONNECTORS

P6 pinout with 3X20 is as follows:

<b>7I68 I/O</b>	<b>3X20 I/O</b>	<b>FPGA BALL</b>	<b>P6 PIN</b>	<b>VIO GROUP</b>
IO24	IO4	C10	1	LEFT VIO
IO25	IO5	B10	3	LEFT VIO
IO26	IO10	E8	5	LEFT VIO
IO27	IO11	D8	7	LEFT VIO
IO28	IO16	C6	9	LEFT VIO
IO29	IO17	B6	11	LEFT VIO
IO30	IO22	B5	13	LEFT VIO
IO31	IO23	A5	15	LEFT VIO
IO32	IO28	E4	17	LEFT VIO
IO33	IO29	D4	19	LEFT VIO
IO34	IO34	F2	21	LEFT VIO
IO35	IO35	F3	23	LEFT VIO
IO36	IO40	H1	25	LEFT VIO
IO37	IO41	H2	27	LEFT VIO
IO38	IO46	K1	29	LEFT VIO
IO39	IO47	K2	31	LEFT VIO
IO40	IO52	N2	33	FIXED 3.3VIO
IO41	IO53	N1	35	FIXED 3.3VIO
IO42	IO58	R2	37	FIXED 3.3VIO
IO43	IO59	R1	39	FIXED 3.3VIO
IO44	IO64	U3	41	FIXED 3.3VIO
IO45	IO65	U2	43	FIXED 3.3VIO
IO46	IO70	W2	45	FIXED 3.3VIO
IO47	IO71	W1	47	FIXED 3.3VIO

# CONNECTORS

## I/O CONNECTORS

P9 pinout with 3X20 is as follows:

<b>7I68 I/O</b>	<b>3X20 I/O</b>	<b>FPGA BALL P9 PIN</b>		<b>VIO GROUP</b>
IO72	IO72	W22	1	RIGHT VIO
IO73	IO73	Y22	3	RIGHT VIO
IO74	IO78	U21	5	RIGHT VIO
IO75	IO79	U20	7	RIGHT VIO
IO76	IO84	R22	9	RIGHT VIO
IO77	IO85	R21	11	RIGHT VIO
IO78	IO90	N20	13	RIGHT VIO
IO79	IO91	N19	15	RIGHT VIO
IO80	IO96	L21	17	RIGHT VIO
IO81	IO97	L22	19	RIGHT VIO
IO82	IO102	K19	21	RIGHT VIO
IO83	IO103	K20	23	RIGHT VIO
IO84	IO108	H21	25	RIGHT VIO
IO85	IO109	H22	27	RIGHT VIO
IO86	IO114	E21	29	RIGHT VIO
IO87	IO115	E22	31	RIGHT VIO
IO88	IO120	A19	33	FIXED 3.3VIO
IO89	IO121	B19	35	FIXED 3.3VIO
IO90	IO126	B17	37	FIXED 3.3VIO
IO91	IO127	C17	39	FIXED 3.3VIO
IO92	IO132	C16	41	FIXED 3.3VIO
IO93	IO133	D16	43	FIXED 3.3VIO
IO94	IO138	A13	45	FIXED 3.3VIO
IO95	IO139	B13	47	FIXED 3.3VIO

# CONNECTORS

## I/O CONNECTORS

P8 pinout with 3X20 is as follows:

<b>7I68 I/O</b>	<b>3X20 I/O</b>	<b>FPGA BALL P8 PIN</b>		<b>VIO GROUP</b>
IO96	IO74	W21	1	RIGHT VIO
IO97	IO75	W20	3	RIGHT VIO
IO98	IO80	T22	5	RIGHT VIO
IO99	IO81	T21	7	RIGHT VIO
IO100	IO86	P22	9	RIGHT VIO
IO101	IO87	P21	11	RIGHT VIO
IO102	IO92	M22	13	RIGHT VIO
IO103	IO93	M21	15	RIGHT VIO
IO104	IO98	L19	17	RIGHT VIO
IO105	IO99	L20	19	RIGHT VIO
IO106	IO104	J21	21	RIGHT VIO
IO107	IO105	J22	23	RIGHT VIO
IO108	IO110	G21	25	RIGHT VIO
IO109	IO111	G22	27	RIGHT VIO
IO110	IO116	E19	29	RIGHT VIO
IO111	IO117	E20	31	RIGHT VIO
IO112	IO122	A18	33	FIXED 3.3VIO
IO113	IO123	B18	35	FIXED 3.3VIO
IO114	IO128	D17	37	FIXED 3.3VIO
IO115	IO129	E17	39	FIXED 3.3VIO
IO116	IO134	B15	41	FIXED 3.3VIO
IO117	IO135	A15	43	FIXED 3.3VIO
IO118	IO140	C13	45	FIXED 3.3VIO
IO119	IO141	D13	47	FIXED 3.3VIO

# CONNECTORS

## I/O CONNECTORS

P7 pinout with 3X20 is as follows:

<b>7I68 I/O</b>	<b>3X20 I/O</b>	<b>FPGA BALL P7 PIN</b>		<b>VIO GROUP</b>
IO120	IO76	V22	1	RIGHT VIO
IO121	IO77	V21	3	RIGHT VIO
IO122	IO82	T20	5	RIGHT VIO
IO123	IO83	T19	7	RIGHT VIO
IO124	IO88	N22	9	RIGHT VIO
IO125	IO89	N21	11	RIGHT VIO
IO126	IO94	M20	13	RIGHT VIO
IO127	IO95	M19	15	RIGHT VIO
IO128	IO100	K21	17	RIGHT VIO
IO129	IO101	K22	19	RIGHT VIO
IO130	IO106	J18	21	RIGHT VIO
IO131	IO107	J19	23	RIGHT VIO
IO132	IO112	F20	25	RIGHT VIO
IO133	IO113	F21	27	RIGHT VIO
IO134	IO118	D21	29	RIGHT VIO
IO135	IO119	D22	31	RIGHT VIO
IO136	IO124	C18	33	FIXED 3.3VIO
IO137	IO125	D18	35	FIXED 3.3VIO
IO138	IO130	A16	37	FIXED 3.3VIO
IO139	IO131	B16	39	FIXED 3.3VIO
IO140	IO136	A14	41	FIXED 3.3VIO
IO141	IO137	B14	43	FIXED 3.3VIO
IO142	IO142	B12	45	FIXED 3.3VIO
IO143	IO143	C12	47	FIXED 3.3VIO

# CONNECTORS

## DIFFERENTIAL PAIRS

The 7I68 supports LVDS signaling on all I/O pairs, that is all even/odd I/O pins starting with 0 comprise a differential pair on the 7I68. Which FPGA pins can have LVDS capability depends on the specific daughterboard module.

## JTAG CONNECTOR

The 7I68 brings out the 3X2X modules JTAG interface to a 6 pin .1" inline connector P3. Pinout is as follows:

PIN	FUNCTION	PIN	FUNCTION
1	TMS	4	TCK
2	TDI	5	GND
3	TDO	6	2.5V

## PCIE CONNECTOR

The optional PCIE connector (for -MP version 3X2xs') is a standard one lane endpoint connector, Molex PN 74960-3018. The PCIE connector is P1. P1 pinout is as follows:

PIN	SIGNAL	PIN	SIGNAL
A1	PERN0	B1	GND
A2	PERP0	B2	RESV
A3	RESV	B3	/CWAKE
A4	GND	B4	/CPRSNT
A5	CREFLKN	B5	GND
A6	CREFLKP	B6	3.3V
A7	GND	B7	CPWRON
A8	/CPERST	B8	PETN0
A9	GND	B9	PETP0

# OPERATION

## LEDS

The 7I68 has 3 status LEDs, CR3: a RED PWRFAIL LED that indicates that the 3.3V output is out of regulation, CR1: a RED /DONE LED that indicates that the FPGA is not configured, and CR2: a green power on LED.

## IO LEVELS

The FPGA chips used in the 3X2X modules are not 5V tolerant but external bus switch parts are used on the 7I68 to make the I/O pins 5V tolerant. The bus switch parts disconnect the FPGA pins from the I/O pins when the I/O pins are driven to positive voltage levels that would damage the FPGA.

The voltage level that causes disconnect can be selected to be ~4V (3.3V mode) or ~3.3V (5V mode). For most applications, the 3.3V mode should be used. The 5V mode is useful when driving 5V referred loads.

Note that there is no protection against negative input voltages other than the input clamp diodes in the FPGA and bus switches, so negative input voltages must be limited to -.5V

## STARTUP I/O VOLTAGE

After power-up or system reset and before the the FPGA is configured, the FPGAs pull-up resistors will pull all I/O signals to a high level. If the FPGA is used for motion control or controlling devices that could present a hazard when enabled, external circuitry should be designed so that this initial state results in a safe condition.

## POWER SUPPLY

The 7I68 uses a on card switching regulator to supply the 3.3 V power that the module requires. Input power is 5V +-5%, The 5V input power also supplies the I/O connector pin 49 power if 5V is selected for that connector.

## POWER SUPPLY ENABLE

The 3.3V switching regulator on the 7I68 is enabled by the PCIE CPWRON signal. This controls a high side switch that switches the 3.3V regulator input power and the 5V I/O connector power. This will make the 7I68 power up and down with the host computer that drives the PCIE cable. If the 7I68 is to be used in a stand-alone application (no PCIE) or if the 7I68/3X2X module must continue operation when the host is powered down or cable disconnected, the automatic power switching can be disabled by setting W5 to the up position.

# REFERENCE

## SPECIFICATIONS

POWER	MIN	MAX	NOTES:
POWER SUPPLY	4.75V	5.25V	
POWER CONSUMPTION:	----	2A	Depends on FPGA Configuration and external load
MAX 5V CURRENT TO I/O CONNS	---	400 mA	Per Connector
MAX 3.3V CURRENT TO I/O CONNS	---	100 mA	Per Connector
ABSOLUTE MAX I/O PIN VOLTAGE	-.5V	7V	5V tolerant mode
ABSOLUTE MAX I/O PIN VOLTAGE	-.5V	4V	3.3V mode
TEMPERATURE RANGE -C version	0 °C	+70 °C	
TEMPERATURE RANGE -I version	-40 °C	+85 °C	