7I53 MANUAL

12 channel encoder interface + 2 channel RS-422 interface daughtercard

V1.2

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Table of Contents

GENERAL

DESCRIPTION

The 7I53 is a twelve channel encoder interface for Mesas Anything I/O series of FPGA interface cards. In addition to the 12 encoder interfaces, the 7I53 provides two full duplex RS-422 interfaces, one capable of RS-485 operation. The 7I53 is designed for motion control applications.

The 7I53 is designed for high density encoder interfacing with up six 7I53s and up to 72 encoder's supported on our larger FPGA cards. One of the 7I53s serial links supports RS-485 (shared bus) interfaces. Encoder inputs can be TTL or differential on a per input basis. The 7I53 can also supply 5V power to encoders.

The controller connection is a 50 pin header that matches the pinout of Mesa's Anything I/O cards. All buffered I/O is terminated with 3.5 mm pluggable screw terminals (supplied)

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I53 card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side.

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W9	CABLE/AUX 5V POWER	RIGHT = CABLE 5V POWER
W30,W34,W38	ENCODER 0	ALL RIGHT = RS-422
W17,W21,W26	ENCODER 1	ALL RIGHT = RS-422
W4,W8,W13	ENCODER 2	ALL RIGHT = RS-422
W29,W33,W37	ENCODER 3	ALL RIGHT = RS-422
W16,W20,W25	ENCODER 4	ALL RIGHT = RS-422
W3,W7,W12	ENCODER 5	ALL RIGHT = RS-422
W28,W32,W36	ENCODER 6	ALL RIGHT = RS-422
W11,W15,W19	ENCODER 7	ALL RIGHT = RS-422
W2,W6,W11	ENCODER 8	ALL RIGHT = RS-422
W27,W31,W35	ENCODER 9	ALL RIGHT = RS-422
W14,W18,W23	ENCODER 10	ALL RIGHT = RS-422
W1,W5,W10	ENCODER 11	ALL RIGHT = RS-422

TTL/RS-422 ENCODER SELECTION

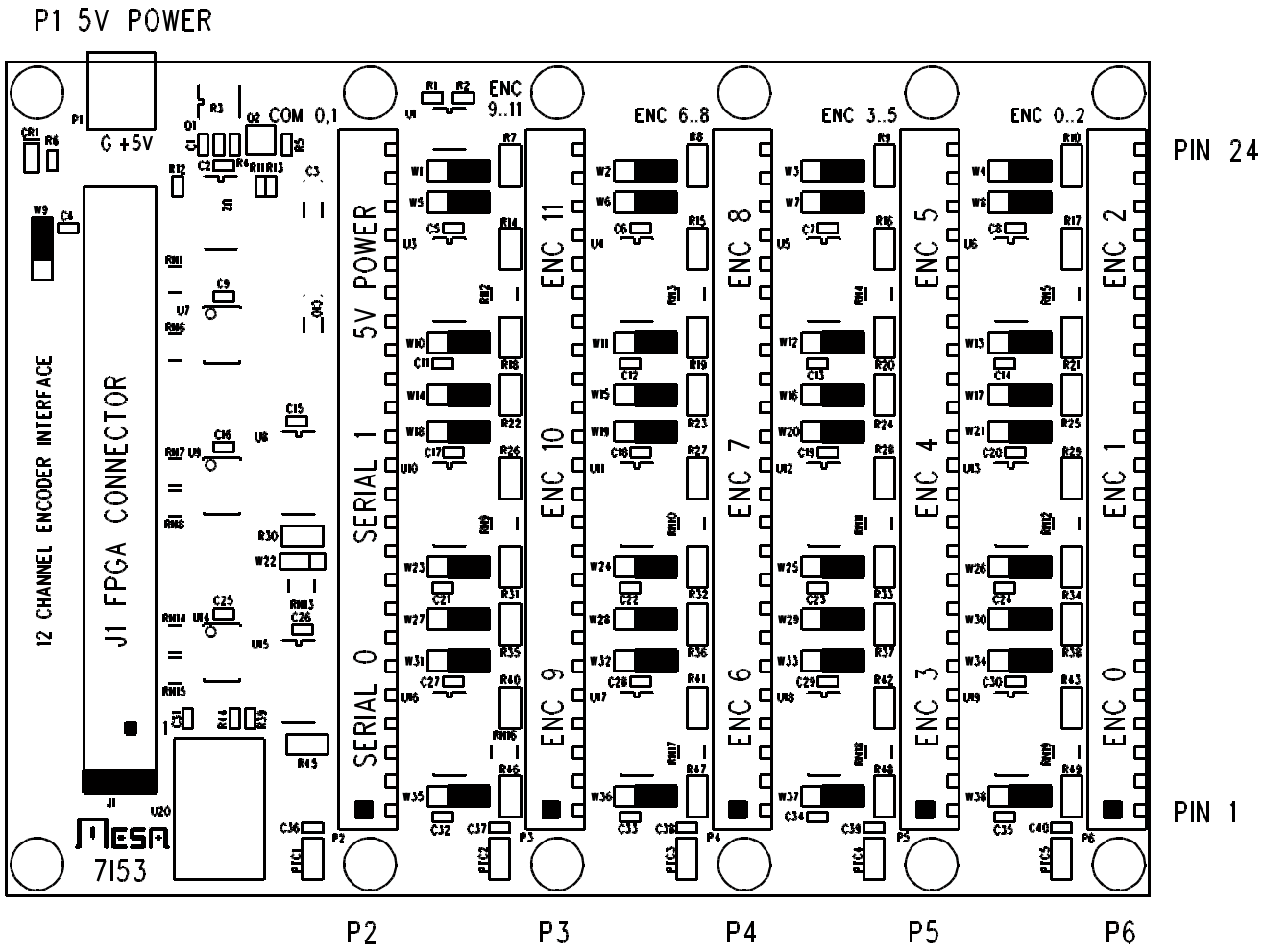
Each 7I53 encoder channel has a selectable TTL or RS-422 (differential) encoder input conditioning. Conditioning type is determined by setting groups of 3 jumpers to the up or down position. When the jumpers are in the "LEFT" position, TTL inputs are selected, When the jumpers are in the "RIGHT" position, RS-422 inputs are selected. Note these sets of three jumpers are in physical proximity to the terminal block encoder connections.

CABLE POWER/P1 POWER SELECTION

The 7I53 can get its operating power from the flat FPGA cable or from P1. For testing and with very low power encoders, cable power can be used. W9 selects whether cable power connects to the 7I53's 5V supply. If W9 is in the "RIGHT" position, cable power is selected. If W9 is in the "LEFT" position, external 5V power must be supplied via P1.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector J1 connects to the Anything I/O card/motion controller. The 7I53 uses multiplexed encoders so each set 3 pins supports 2 encoders.

PIN	FUNCTION	DIRECTION	PIN	FUNCTION	DIRECTION
1	MENCA0	FROM 7I53	25	MENCA4	FROM 7I53
3	MENCB0	FROM 7I53	27	MENCB4	FROM 7I53
5	MIDX0	FROM 7I53	29	MIDX4	FROM 7I53
7	MENCA1	FROM 7I53	31	MENCA5	FROM 7I53
9	MENCB1	FROM 7I53	33	MENCB5	FROM 7I53
11	MIDX1	FROM 7I53	35	MIDX5	FROM 7I53
13	MENCA2	FROM 7I53	37	ENCMUX	TO 7I53
15	MENCB2	FROM 7I53	39	RX0	FROM 7I53
17	MIDX2	FROM 7I53	41	TX0	TO 7I53
19	MENCA3	FROM 7I53	43	RX1	FROM 7I53
21	MENCB3	FROM 7I53	45	TX1	TO 7I53
23	MIDX3	FROM 7I53	47	TXEN1	TO 7I53
			49	+5V PWR	TO 7I53

Note: all even pins are grounded. Alternate encoder names omitted for space. The ‘M’ prefix on the interface encoder signals is to indicate that they are multiplexed signals.

AUX 5V POWER

2 pin pluggable terminal P1 can be used to supply 5V power to the I/O terminals on the7I53. This is suggested for most applications as the encoders typically will draw more current than can be supplied via the FPGA flat cable. P1 has the following pinout:

PIN	FUNCTION
1	5V
2	GND

CONNECTORS

ENCODER CONNECTOR P6

Connector P6 is a 3.5MM pluggable screw terminal block with encoder channels 0 through 2:

P5 PIN	FUNCTION	DIR
1	QA0	TO 7I53
2	/QA0	TO 7I53
3	GND	FROM 7I53
4	QB0	TO 7I53
5	/QB0	TO 7I53
6	+5V	FROM 7I53
7	IDX0	TO 7I53
8	/IDX0	TO 7I53
9	QA1	TO 7I53
10	/QA1	TO 7I53
11	GND	FROM 7I53
12	QB1	TO 7I53
13	/QB1	TO 7I53
14	+5V	FROM 7I53
15	IDX1	TO 7I53
16	/IDX1	TO 7I53
17	QA2	TO 7I53
18	/QA2	TO 7I53
19	GND	FROM 7I53
20	QB2	TO 7I53
21	/QB2	TO 7I53
22	+5V	FROM 7I53
23	IDX2	TO 7I53
24	/IDX2	TO 7I53

Note that actual signal functions depend on FPGA configuration.

CONNECTORS

ENCODER CONNECTOR P5

Connector P5 is a 3.5MM pluggable screw terminal block with the following pinout:

P3 PIN	FUNCTION	DIR
1	QA3	TO 7I53
2	/QA3	TO 7I53
3	GND	FROM 7I53
4	QB3	TO 7I53
5	/QB3	TO 7I53
6	+5V	FROM 7I53
7	IDX3	TO 7I53
8	/IDX3	TO 7I53
9	QA4	TO 7I53
10	/QA4	TO 7I53
11	GND	FROM 7I53
12	QB4	TO 7I53
13	/QB4	TO 7I53
14	+5V	FROM 7I53
15	IDX4	TO 7I53
16	/IDX4	TO 7I53
17	QA5	TO 7I53
18	/QA5	TO 7I53
19	GND	FROM 7I53
20	QB5	TO 7I53
21	/QB5	TO 7I53
22	+5V	FROM 7I53
23	IDX5	TO 7I53
24	/IDX5	TO 7I53

Note that actual signal functions depend on FPGA configuration.

CONNECTORS

ENCODER CONNECTOR P4

Connector P4 is a 3.5MM pluggable screw terminal block with the following pinout:

P3 PIN	FUNCTION	DIR
1	QA6	TO 7I53
2	/QA6	TO 7I53
3	GND	FROM 7I53
4	QB6	TO 7I53
5	/QB6	TO 7I53
6	+5V	FROM 7I53
7	IDX6	TO 7I53
8	/IDX6	TO 7I53
9	QA7	TO 7I53
10	/QA7	TO 7I53
11	GND	FROM 7I53
12	QB7	TO 7I53
13	/QB7	TO 7I53
14	+5V	FROM 7I53
15	IDX7	TO 7I53
16	/IDX7	TO 7I53
17	QA8	TO 7I53
18	/QA8	TO 7I53
19	GND	FROM 7I53
20	QB8	TO 7I53
21	/QB8	TO 7I53
22	+5V	FROM 7I53
23	IDX8	TO 7I53
24	/IDX8	TO 7I53

Note that actual signal functions depend on FPGA configuration

CONNECTORS

ENCODER CONNECTOR P3

Connector P3 is a 3.5MM pluggable screw terminal block with the following pinout:

P3 PIN	FUNCTION	DIR
1	QA9	TO 7I53
2	/QA9	TO 7I53
3	GND	FROM 7I53
4	QB9	TO 7I53
5	/QB9	TO 7I53
6	+5V	FROM 7I53
7	IDX9	TO 7I53
8	/IDX9	TO 7I53
9	QA10	TO 7I53
10	/QA10	TO 7I53
11	GND	FROM 7I53
12	QB10	TO 7I53
13	/QB10	TO 7I53
14	+5V	FROM 7I53
15	IDX10	TO 7I53
16	/IDX10	TO 7I53
17	QA11	TO 7I53
18	/QA11	TO 7I53
19	GND	FROM 7I53
20	QB11	TO 7I53
21	/QB11	TO 7I53
22	+5V	FROM 7I53
23	IDX11	TO 7I53
24	/IDX11	TO 7I53

Note that actual signal functions depend on FPGA configuration

CONNECTORS

RS-422 INTERFACE CONNECTOR P3

Connector P3 is a 3.5MM pluggable screw terminal block with the following pinout:

P3 PIN	FUNCTION	DIR
1	GND	FROM 7I53
2	GND	FROM 7I53
3	RX0	TO 7I53
4	/RX0	TO 7I53
5	TX0	FROM 7I53
6	/TX0	FROM 7I53
7	+5V	FROM 7I53
8	+5V	FROM 7I53
9	GND	FROM 7I53
10	GND	FROM 7I53
11	RX1	TO 7I53
12	/RX1	TO 7I53
13	TX1	FROM 7I53
14	/TX1	FROM 7I53
15	+5V	FROM 7I53
16	+5V	FROM 7I53
17	GND	FROM 7I53
18	GND	FROM 7I53
19	NC	
20	NC	
21	NC	
22	NC	
23	+5V	FROM 7I53
24	+5V	FROM 7I53

Note that actual signal functions depend on FPGA configuration.

OPERATION

5V POWER

The 7I53 requires ~500 mA of 5V power for operation. This power will increase based on the number of terminated TX outputs used, up to a maximum of ~700 mA of local logic power. Encoder power and remote serial device power must be added to this figure for total power draw.

Power for the 7I53 logic is normally supplied from P1, the AUX 5V power connector. The 7I53 incorporates a high-side power switch to enable 5V power to all logic and I/O connectors only when 5V cable power is present. This allows the 7I53s AUX 5V power to be supplied continuously to P1 without the risk of reverse powering the FPGA card when the PC is turned off.

If W9 is on the "UP" position, the controller cable will supply both the logic and I/O power and P1 can remain unconnected. This mode can be used for testing with perhaps a single encoder and single RS-422 channel, but it is suggested that W9 be placed in the "DOWN" position and I/O power be supplied via P1 for most applications.

The 5V power to I/O connectors P2,P3,P4,P5 and P6 each pass through a 1.1A PTC device before being routed to the I/O terminals. This limits the I/O power supplied by P2, P3,P4,P5 and P6 to ~640 mA each in 0 to 70C ambients.

ENCODER INPUT CIRCUIT

The 7I53 input circuit is different depending on whether TTL or RS-422 encoder types have been selected. In TTL mode the input circuit on the encoder QA, QB, and IDX inputs drive one input of the RS-422 differential receiver, and the other receiver input is terminated to a 1.6V (TTL threshold) reference voltage. In RS-422 mode, the input consists of a 120 Ohm termination resistor and a 26LS32 RS-422 differential receiver.

When TTL encoders are used, they connect to the ‘True’ input of the differential pair, for example a TTL encoder for channel 2 would connect to QA2, QB2 and IDX2, while the /QA2, /QB2, and /IDX2 terminals would be left open.

Fine print: normally the input mode jumpers would always be moved as a sets of three to select TTL or RS-422 mode for individual encoders, however it is possible to select TTL or RS-422 mode for each encoder signal, for example if a encoder had a differential A, B but TTL index, the input circuit can accommodate this. The three input mode select jumpers are in bottom to top order: QA, QB, IDX.

OPERATION

MAXIMUM ENCODER COUNT RATE

The 7I53 uses multiplexed encoder signals to save interface pins. The multiplexing rate will determine the maximum encoder count rate. Default multiplexing rate with HostMot2 firmware is ClockLow / 8,or approximately 4 or 6 MHz, giving a resolvable count rate of 2 to 3 MHz. Multiplexing rate can be increased if desired but high multiplex rates will require short cables between the FPGA controller card and the 7I53 due to signal integrity and time-of-flight considerations. Maximum practical multiplex rate is approximately 12 MHz (and 6 MHz count rates). Encoder count rate is further limited by HostMot2s input filtering to ~5 to ~8 million counts per second (encoder filtering off) and ~1 to ~1.6 million counts per second (encoder filtering on).

RS-485 CAPABLE CHANNEL

One of the serial channels on the 7I53 has an output enable function and can be used for RS-485 type applications. This is channel 1. For two wire half duplex type RS-485 interfaces, the RX+ and TX+ lines and the RX- and TX- lines should be tied together.

INTERFACING WITH MESA SERIAL DEVICES

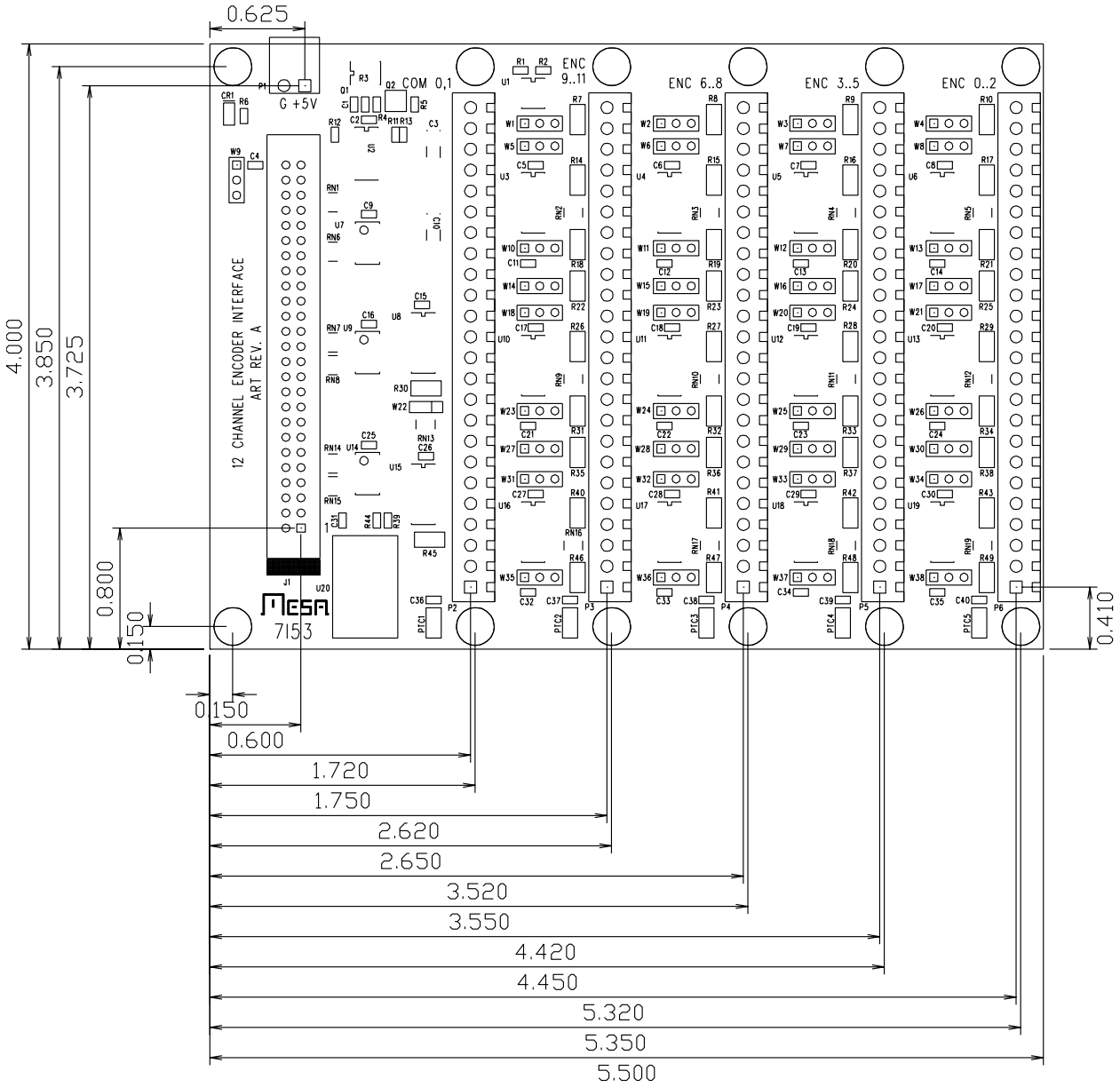
The 7I53 in intended to be a general purpose RS-422 serial plus encoder interface but can easily interface to MESA's serial I/O devices that use RS-422 communication and RJ45/CAT5 cable for the serial interface. These devices include the 7I64 Isolated I/O interface, the 8I20 3 phase drive, the 7I66 isolated I/O interface, the 7I69 TTL I/O interface and the 7I73 pendant interface. The easiest way to make a cable for interfacing the 7I53 to these devices is to take a standard CAT5 or CAT6 cable, cut it in half, and wire the individual wires to the 7I53 screw terminals. The following chart gives the CAT5 to 7I53 screw terminal connections (EIA/TIA 568B colors shown):

7I53 P2 PIN	7I53 P2SIGNAL	DIRECTION	CAT5 PIN	CAT5 568B COLOR
1,9	GND	FROM 7I53	4	BLUE
2,10	GND	FROM 7I53	5	BLUE / WHITE
3,11	RX+	TO 7I53	6	GREEN
4,12	RX-	TO 7I53	3	GREEN / WHITE
5,13	TX+	FROM 7I53	2	ORANGE
6,14	TX-	FROM 7I53	1	ORANGE / WHITE
7,15	+5V	FROM 7I53	7	BROWN / WHITE
8,16	+5V	FROM 7I53	8	BROWN

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.75	5.25	VDC
5V POWER CONSUMPTION	---	700	mA
(all outputs loaded with 130 ohm terminations)			
(no external encoder or serial 5V load)			
5V CURRENT TO EACH I/O CONNECTOR	---	640	mA
MAXIMUM RS-422 DATA RATE	---	10	MBIT/S
RS-422 INPUT COMMON MODE RANGE	-7	+12	Volts
RS-422 TERMINATION RESISTANCE	118	122	Ohm
RS-422 OUTPUT LOW	—	.8	Volts
(24 mA sink current)			
RS-422 OUTPUT HIGH	VCC-2.5	—	Volts
(24 mA source current)			
ENC INPUT COMMON MODE RANGE	-7	+12	Volts
ENC INPUT TTL MODE THRESHOLD	1.4	1.8	Volts
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND

DRAWINGS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3.725
0.800
0.150
0.410
0.150
0.600
1.720
1.750
2.620
2.650
3.520
3.550
4.420
4.450
5.320
5.350
5.500
12 CHANNEL ENCODER INTERFACE
ART REV. A
7I53
G +5V
COM 0,1
ENC 9..11
ENC 6..8
ENC 3..5
ENC 0..2
P1
P2
P3
P4
P5
P6
J1