7I52S MANUAL

12 channel differential output + 6 channel encoder interface

V1.5

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GENERAL

DESCRIPTION

The 7I52 is a 12 channel differential output plus six channel encoder interface for Mesas Anything I/O series of FPGA interface cards. The 7I52 is designed for motion control applications.

A common usage of the 7I52S would be connecting up to six Step+Dir or PWM+Dir drives to the 7I52S's differential outputs and up to six encoders with index to the 7I52S's encoder inputs. The 7I52S's differential outputs swing a full 5V and will drive 20 mA loads.

The controller connection is a 50 pin header that matches the pinout of Mesa's Anything I/O cards. All buffered I/O is terminated with 3.5 mm pluggable screw terminals (supplied)

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I52S card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side.

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W3	CABLE/EXT 5V POWER	LEFT = EXT 5V POWER
W15,W18,W20	ENCODER 0	ALL DOWN = RS-422
W9,W11,W13	ENCODER 1	ALL DOWN = RS-422
W2,W5,W7	ENCODER 2	ALL DOWN = RS-422
W14,W17,W19	ENCODER 3	ALL DOWN = RS-422
W8,W10,W12	ENCODER 4	ALL DOWN = RS-422
W1,W4,W6	ENCODER 5	ALL DOWN = RS-422

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TTL/RS-422 ENCODER SELECTION

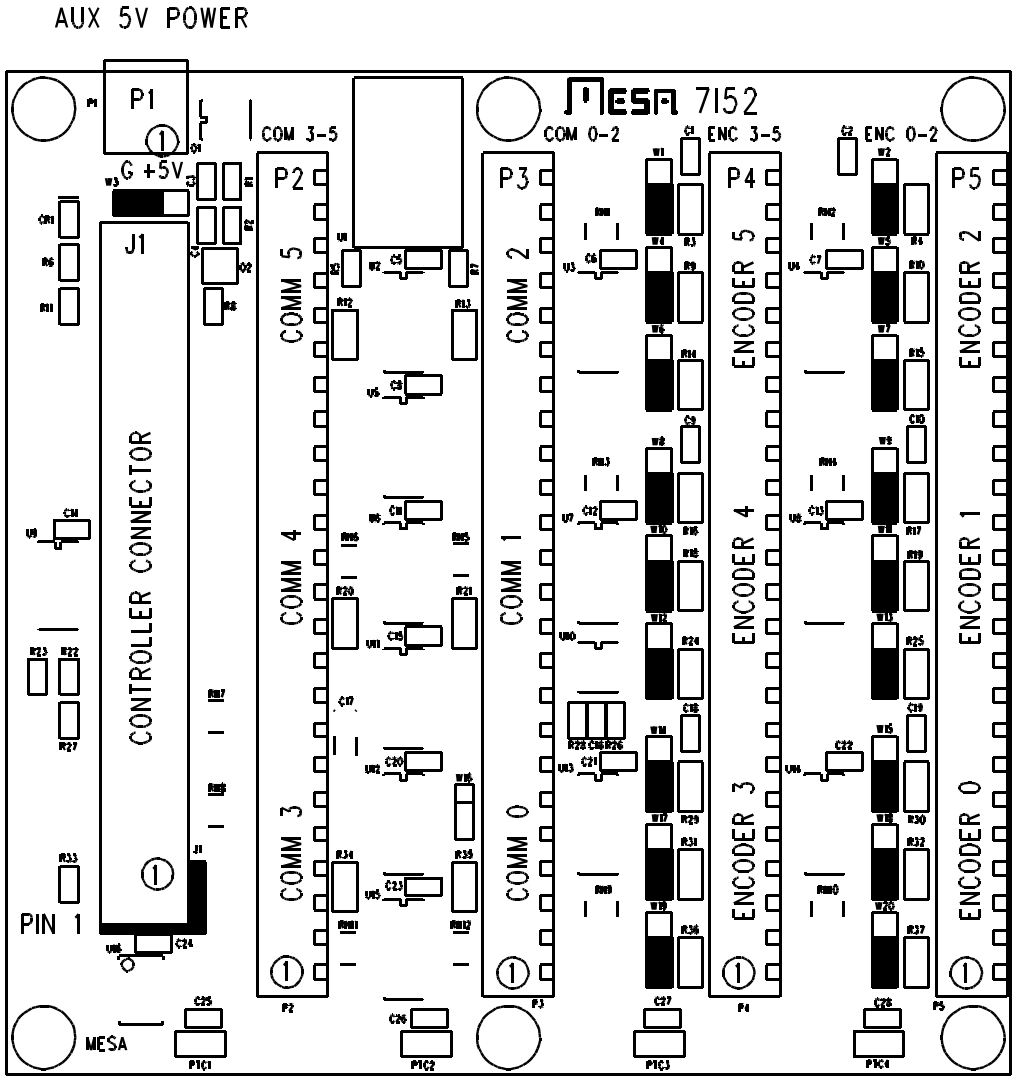
Each 7I52S encoder channel has a selectable TTL or RS-422 (differential) encoder input conditioning. Conditioning type is determined by setting groups of 3 jumpers to the up or down position. When the jumpers are in the "UP" position, TTL inputs are selected, When the jumpers are in the "DOWN" position, RS-422 inputs are selected. Note these sets of three jumpers are in physical proximity to the terminal block encoder connections.

CABLE POWER/P1 POWER SELECTION

The 7I52S can get its operating power from the flat FPGA cable or from P1. For testing and with very low power encoders, cable power can be used. W3 selects whether cable power connects to the 7I52S's 5V supply. If W3 is in the "RIGHT" position, cable power is selected. If W3 is in the "LEFT" position, external 5V power must be supplied via P1.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector J1 connects to the anything I/O card/motion controller. This can be a male 50 pin header on the top of the 7I52S card or a female 50 conductor header on the bottom side of the 7I52S depending on 7I52S model.

PIN	FUNCTION	DIRECTION	PIN	FUNCTION	DIRECTION
1	/TX3BENA	TO 7I52S	25	TX5A	TO 7I52S
3	MENCA0	FROM 7I52S	27	TX4B	TO 7I52S
5	MENCB0	FROM 7I52S	29	TX4A	TO 7I52S
7	MIDX0	FROM 7I52S	31	TX3B	TO 7I52S
9	MENCA1	FROM 7I52S	33	TX3A	TO 7I52S
11	MENCB1	FROM 7I52S	35	TX2B	TO 7I52S
13	MIDX1	FROM 7I52S	37	TX2A	TO 7I52S
15	MENCA2	FROM 7I52S	39	TX1B	TO 7I52S
17	MENCB2	FROM 7I52S	41	TX1A	TO 7I52S
19	MIDX2	FROM 7I52S	43	TX0B	TO 7I52S
21	ENCMUX	TO 7I52S	45	TX0A	TO 7I52S
23	TX5B	TO 7I52S	47	/TX0BENA	TO 7I52S
			49	+5V PWR	TO 7I52S

Note: all even pins are grounded. Alternate encoder names omitted for space. The ‘M’ prefix on the interface encoder signals is to indicate that they are multiplexed signals.

EXT 5V POWER

2 pin pluggable terminal P1 can be used to supply 5V power to the I/O terminals on the 7I52S. This is suggested for most applications as the encoders typically will draw more current than can be supplied via the FPGA flat cable. P1 has the following pinout:

PIN	FUNCTION
1	5V
2	GND

CONNECTORS

ENCODER CONNECTOR P5

Connector P5 is a 3.5MM pluggable screw terminal block with encoder channels 0 through 2:

P5 PIN	FUNCTION	DIR
1	QA0	TO 7I52S
2	/QA0	TO 7I52S
3	GND	FROM 7I52S
4	QB0	TO 7I52S
5	/QB0	TO 7I52S
6	+5V	FROM 7I52S
7	IDX0	TO 7I52S
8	/IDX0	TO 7I52S
9	QA1	TO 7I52S
10	/QA1	TO 7I52S
11	GND	FROM 7I52S
12	QB1	TO 7I52S
13	/QB1	TO 7I52S
14	+5V	FROM 7I52S
15	IDX1	TO 7I52S
16	/IDX1	TO 7I52S
17	QA2	TO 7I52S
18	/QA2	TO 7I52S
19	GND	FROM 7I52S
20	QB2	TO 7I52S
21	/QB2	TO 7I52S
22	+5V	FROM 7I52S
23	IDX2	TO 7I52S
24	/IDX2	TO 7I52S

Note that actual signal functions depend on FPGA configuration.

CONNECTORS

ENCODER CONNECTOR P4

Connector P4 is a 3.5MM pluggable screw terminal block with the following pinout:

P3 PIN	FUNCTION	DIR
1	QA3	TO 7I52S
2	/QA3	TO 7I52S
3	GND	FROM 7I52S
4	QB3	TO 7I52S
5	/QB3	TO 7I52S
6	+5V	FROM 7I52S
7	IDX3	TO 7I52S
8	/IDX3	TO 7I52S
9	QA4	TO 7I52S
10	/QA4	TO 7I52S
11	GND	FROM 7I52S
12	QB4	TO 7I52S
13	/QB4	TO 7I52S
14	+5V	FROM 7I52S
15	IDX4	TO 7I52S
16	/IDX4	TO 7I52S
17	QA5	TO 7I52S
18	/QA5	TO 7I52S
19	GND	FROM 7I52S
20	QB5	TO 7I52S
21	/QB5	TO 7I52S
22	+5V	FROM 7I52S
23	IDX5	TO 7I52S
24	/IDX5	TO 7I52S

Note that actual signal functions depend on FPGA configuration.

CONNECTORS

DIFFERENTIAL OUTPUT CONNECTOR P3

Connector P3 is a 3.5MM pluggable screw terminal block with the following pinout:

P3 PIN	FUNCTION	DIR
1	GND	FROM 7I52S
2	GND	FROM 7I52S
3	TX0A	FROM 7I52S
4	/TX0A	FROM 7I52S
5	TX0B	FROM 7I52S
6	/TX0B	FROM 7I52S
7	+5V	FROM 7I52S
8	+5V	FROM 7I52S
9	GND	FROM 7I52S
10	GND	FROM 7I52S
11	TX1A	FROM 7I52S
12	/TX1A	FROM 7I52S
13	TX1B	FROM 7I52S
14	/TX1B	FROM 7I52S
15	+5V	FROM 7I52S
16	+5V	FROM 7I52S
17	GND	FROM 7I52S
18	GND	FROM 7I52S
19	TX2A	FROM 7I52S
20	/TX2A	FROM 7I52S
21	TX2B	FROM 7I52S
22	/TX2B	FROM 7I52S
23	+5V	FROM 7I52S
24	+5V	FROM 7I52S

Note that actual signal functions depend on FPGA configuration.

CONNECTORS

DIFFERENTIAL OUTPUT CONNECTOR P2

Connector P2 is a 3.5MM pluggable screw terminal block with the following pinout:

P2 PIN	FUNCTION	DIR
1	GND	FROM 7I52S
2	GND	FROM 7I52S
3	TX3A	FROM 7I52S
4	/TX3A	FROM 7I52S
5	TX3B	FROM 7I52S
6	/TX3B	FROM 7I52S
7	+5V	FROM 7I52S
8	+5V	FROM 7I52S
9	GND	FROM 7I52S
10	GND	FROM 7I52S
11	TX4A	FROM 7I52S
12	/TX4A	FROM 7I52S
13	TX4B	FROM 7I52S
14	/TX4B	FROM 7I52S
15	+5V	FROM 7I52S
16	+5V	FROM 7I52S
17	GND	FROM 7I52S
18	GND	FROM 7I52S
19	TX5A	FROM 7I52S
20	/TX5A	FROM 7I52S
21	TX5B	FROM 7I52S
22	/TX5B	FROM 7I52S
23	+5V	FROM 7I52S
24	+5V	FROM 7I52S

Note that actual signal functions depend on FPGA configuration.

OPERATION

5V POWER

The 7I52S requires ~200 mA of 5V power for operation. This power will increase based on the number of terminated differential outputs used, up to a maximum of ~400 mA of local logic power. Encoder power and remote serial device power must be added to this figure for total power draw

Power for the 7I52S logic is normally supplied from P1, the EXT 5V power connector. The 7I52S incorporates a high-side power switch to enable 5V power to all logic and I/O connectors only when 5V cable power is present. This allows the 7I52Ss EXT 5V power to be supplied continuously to P1 without the risk of reverse powering the FPGA card when the PC is turned off.

If W3 is on the right hand position, the controller cable will supply both the logic and I/O power and P1 can remain unconnected. This mode can be used for testing with perhaps a single encoder and single differential output channel, but it is suggested that W3 be placed in the left hand position and I/O power be supplied via P1 for most applications.

The 5V power to I/O connectors P2,P3,P4 and P5 each pass through a 1.1A PTC device before being routed to the I/O terminals. This limits the I/O power supplied by P2, P3,P4 and P5 to ~640 mA each in 0 to 70C ambient temperature environment.

ENCODER INPUT CIRCUIT

The 7I52S input circuit is different depending on whether TTL or RS-422 encoder types have been selected. In TTL mode the input circuit on the encoder QA, QB, and IDX inputs drive one input of the RS-422 differential receiver, and the other receiver input is terminated to a 1.6V (TTL threshold) reference voltage. In RS-422 mode, the input consists of a 120 Ohm termination resistor and a 26LS32 RS-422 differential receiver.

When TTL encoders are used, they connect to the 'True' input of the differential pair, for example a TTL encoder for channel 2 would connect to QA2, QB2 and IDX2, while the /QA2, /QB2, and /IDX2 terminals would be left open.

Fine print: normally the input mode jumpers would always be moved as a sets of three to select TTL or RS-422 mode for individual encoders, however it is possible to select TTL or RS-422 mode for each encoder signal, for example if a encoder had a differential A, B but TTL index, the input circuit can accommodate this. The three input mode select jumpers are in bottom to top order: QA, QB, IDX.

OPERATION

MAXIMUM ENCODER COUNT RATE

The 7I52S uses multiplexed encoder signals to save interface pins. The multiplexing rate will determine the maximum encoder count rate. Default multiplexing rate with HostMot2 firmware is ClockLow / 8,or approximately 4 or 6 MHz, giving a resolvable count rate of 2 to 3 MHz. Multiplexing rate can be increased if desired but high multiplex rates will require short cables between the FPGA controller card and the 7I52S due to signal integrity and time-of-flight considerations. Maximum practical multiplex rate is approximately 12 MHz (and 6 MHz count rates). Encoder count rate is further limited by HostMot2s input filtering to ~5 to ~8 million counts per second (encoder filtering off) and ~1 to ~1.6 million counts per second (encoder filtering on).

DIFFERENTIAL OUTPUT DRIVE

The 7I52S outputs are designed to drive singly terminated RS-422 lines or remote opto-isolator diodes. Maximum output drive is 35 mA. The 7I52S outputs can be used individually for interfacing single ended loads. Unloaded outputs swing to 5V (Full 5V CMOS outputs)

TX0B AND TX3B ENABLE

Differential outputs TX0B and TX3B can be tri-stated (floated). To enable outputs TX0B and /TX0B, /TX0BENA must be driven low by the FPGA. To enable outputs TX3B and /TX3B, /TX3BENA must be driven low by the FPGA.

STARTUP OUTPUT POLARITY AND STATE

When 7I52S outputs are used for drive enables or other safety related controls its very important that the startup state disables the external equipment.

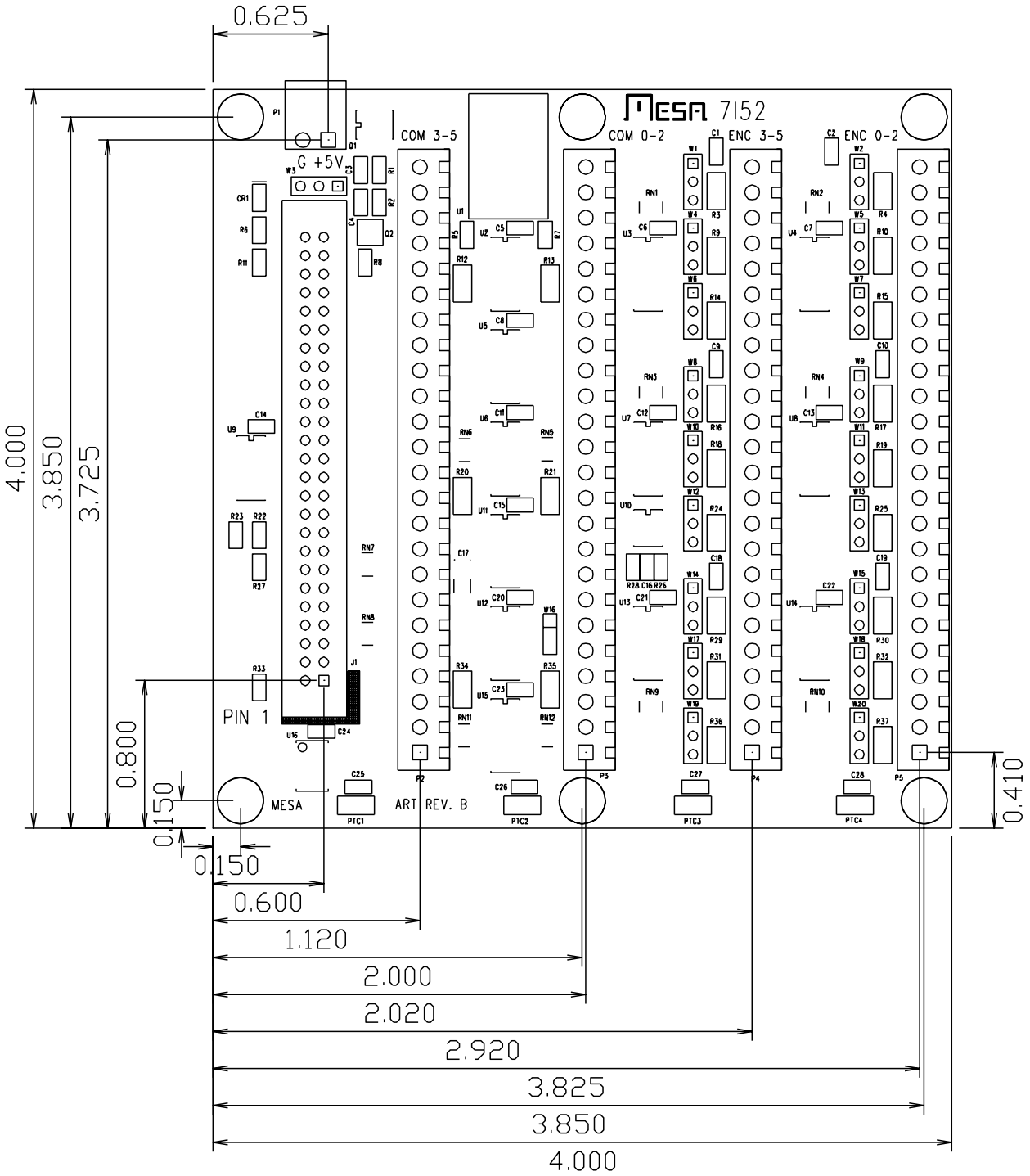
The differential outputs are polarized such that the TXNA and TXNB pins are inverted from the FPGA pins and the /TXNA and /TXNB pins are non inverting. This may seem a little backwards but it's an artifact of the communication oriented background of the 7I52S. Since the FPGA cards outputs are high at startup, the TXNA and TXNB pins will be low at startup (and therefore suitable for active high enables). The /TXNA and /TXNB pins will be high at startup (and suitable for active low enables)

Note that until /TX0BENA and /TX3BENA are asserted low by the host, TXB0, /TXB0, TXB3 and /TXB3 will float. If TXB0, /TXB0, TXB3 or /TXB3 are used as enables, external equipment must be disabled when the input is not driven.

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.75	5.25	VDC
5V POWER CONSUMPTION	---	400	mA
(all outputs loaded with 130 ohm terminations)			
(no external encoder or serial 5V load)			
5V CURRENT TO EACH I/O CONNECTOR	---	640	mA
MAXIMUM DATA OUTPUT RATE	---	10	MBIT/S
RS-422 OUTPUT LOW	—	.8	Volts
(24 mA sink current)			
RS-422 OUTPUT HIGH	VCC-2.5	—	Volts
(24 mA source current)			
ENC INPUT COMMON MODE RANGE	-7	+12	Volts
ENC INPUT TTL MODE THRESHOLD	1.4	1.8	Volts
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND

DRAWINGS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3.850
4.000
0.410
MESA 7I52
COM 3-5
COM 0-2
ENC 3-5
ENC 0-2
+5V
PIN 1
MESA
ART REV. B
P1
P2
P3
P4
P5
J1