7I50 MANUAL

24 I/O SPI EXPANDER

V1.0

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GENERAL

DESCRIPTION

The 7I50 is an 24 I/O SPI expander designed for high speed I/O expansion of Mesa's Anything I/O cards. The SPI interface is compatible with Mesas Anything I/O cards and supports high speed real time I/O. An differential (RS-422) SPI option allows long 7I50 to host cable lengths.

A SPI breakout card (7I46) allows up to six 7I50s to connect to a single 50 pin Anything I/O connector. The SPI interface supports data rates to 8 Mbps with 5 foot cables so a full read/write of all 24 I/O bits takes approximately 4 uSec. Outputs are 5V open drain with 3.3K pull-ups. Outputs will sink 15 mA. A built in watchdog timer sets the outputs to a inactive level if not accessed within a presettable watchdog interval. The I/O connector is a 50 pin header, compatible with Opto 22 I/O module racks and low speed Anything I/O daughter cards.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I50 card is oriented in an upright position, that is, with the MESA logo on the top and the 50 pin I/O header on the right.

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W1	SPI INTERFACE SELECT	RIGHT = TTL
W2,W3	WATCHDOG TIMEOUT	LEFT,RIGHT = 210 MS

SPI INTERFACE SELECTION

The 7I50 can use a TTL (default) or differential SPI interface to the host. When W1 is in the right hand position, the TTL SPI interface (10 pin connector P4) is selected. When W1 is in the left hand position, the differential interface (16 pin connector P2) is selected.

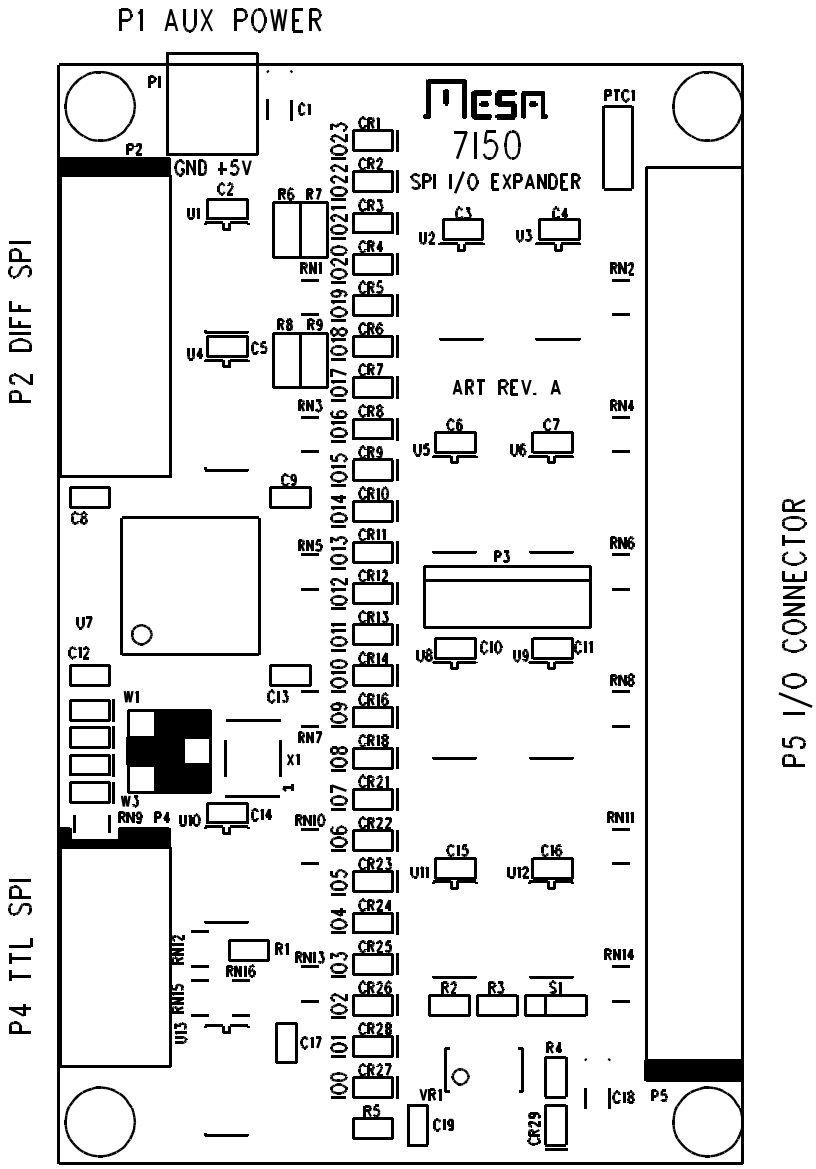
WATCHDOG TIMEOUT SELECTION

The 7I50 incorporates a watchdog circuit to disable (set high) all 24 outputs when the host interface has not updated the output register for a selectable period of time. The timeout period is selectable via jumpers W2 and W3.

W2	W3	TIMEOUT
RIGHT	RIGHT	13 MS
RIGHT	LEFT	52 MS
LEFT	RIGHT	210 MS
LEFT	LEFT	WATCHDOG DISABLED

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

TTL SPI CONNECTOR

10 pin header connector P4 is the TTL level SPI interface connector. P4 can also supply power to the 7I50 as long as the cable length is less than 10 feet. This assumes the 7I50 does not power additional devices from its I/O connector. The 7I46 breakout card allows up to six 7I50s to connect to a single "Anything I/O" connector.

PIN	FUNCTION	DIRECTION
1	+5V	TO 7I50
2	GND	TO 7I50
3	/CS	TO 7I50
4	GND	TO 7I50
5	SDI	TO 7I50
6	GND	TO 7I50
7	SCLK	TO 7I50
8	GND	TO 7I50
9	SDO	FROM 7I50
10	+5V	TO 7I50

CONNECTORS

DIFFERENTIAL SPI CONNECTOR

16 pin header connector P2 is the differential level SPI interface connector. P2 can also supply power to the 7I50 as long as the cable length is less than 5 feet. The 7I46D breakout card allows up to six 7I50s to connect to a single "Anything I/O" connector

PIN	FUNCTION	DIRECTION
1	+5V	TO 7I50
2	+/CS	TO 7I50
3	-/CS	TO 7I50
4	GND	TO 7I50
5	+SDI	TO 7I50
6	-SDI	TO 7I50
7	GND	TO 7I50
8	+SDO	FROM 7I50
9	-SDO	FROM 7I50
10	GND	TO 7I50
11	+SCLK	TO 7I50
12	-SCLK	TO 7I50
13	GND	TO 7I50
14	+SPARE	TO 7I50
15	-SPARE	TO 7I50
16	+5V	TO 7I50

AUX 5V POWER

Two pin 3.5 mm connector P1 is normally used to supply 5V power to the 7I50 when not powered via the SPI connectors, or when the SPI cable length is too great to supply sufficient power. P1 has the following pin-out:

PIN	FUNCTION
1	5V (SQUARE PAD)
2	GND

CONNECTORS

I/O CONNECTOR

P5 is the 7I50s I/O connector. P5 is a 50 pin box header that mates with standard 50 conductor female IDC connectors. Suggested compatible IDC receptacle is AMP PN 1-1658621-0. 7I50 IO connector pinouts are as follows:

P5 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO0	2	GND	3	IO1	4	GND
5	IO2	6	GND	7	IO3	8	GND
9	IO4	10	GND	11	IO5	12	GND
13	IO6	14	GND	15	IO7	16	GND
17	IO8	18	GND	19	IO9	20	GND
21	IO10	22	GND	23	IO11	24	GND
25	IO12	26	GND	27	IO13	28	GND
29	IO14	30	GND	31	IO15	32	GND
33	IO16	34	GND	35	IO17	36	GND
37	IO18	38	GND	39	IO19	40	GND
41	IO20	42	GND	43	IO21	44	GND
45	IO22	46	GND	47	IO23	48	GND
49	POWER	50	GND				

OPERATION

SPI INTERFACE

The 7I50 host interface is via SPI. SPI data format is MSB first, with 32 data bits:

SPI DATA BITS 31 .. 24

COM3	COM2	COM1	COM0	WHB	XX	XX	XX

SPI DATA BITS 23 .. 16

I/O23	I/O22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16

SPI DATA BITS 15 .. 8

I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8

SPI DATA BITS 7 .. 0

I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0

The most significant bits of the SPI data, bits 28,29,30, and 31 are the command bits. The command bits determine if the SPI operation is a read or write. A command of 0xA is a write and a command of 0xB is a read. Other commands are invalid and will clear any outputs and set the watchdog has bitten flag. Bit 27 is the Watchdog_Has_Bitten flag (WHB). On a read command, a one in this bit indicates that the 7I50s watchdog has bitten. On a write if this bit is a one, the watchdog has bitten flag will be cleared. A write command always echos the input data, so a single SPI cycle can be used to both update the outputs and read the inputs.

Note that a write command will fail if the WatchDog_Has_Bitten flag is set. This means that initialization and error recovery code must first clear the WHB bit before writing data to the 7I50. It is suggested that normal write code not clear the WHB flag as this creates a race condition and watchdog timeout could be missed.

OPERATION

SPI INTERFACE SETTINGS

The SPI interface will support SPI clock rate up to 8 MHz. This assumes a 5 foot maximum controller cable length. For use with Mesa HostMot2 configuration SPI interfaces (SSPI or BSPI), channel setup is as follows:

CPOL	= 0
CPHA	= 1
BITS PER FRAME	= 0x1F (For 32 bits)
SPI BIT RATE	= 1 for 33MHz ClockLow FPGAs =
	= 2 for ~50 MHz ClockLow FPGAs.
	= 5 for ~100 MHz ClockLow FPGAs
	This results in a ~ 8MHZ SPI clock = ClockLow/(2*(bitrate+1))

For longer cables and differential mode it may be necessary to run the SPI clock at a lower frequency. A 3 MHz SPI clock will work with differential SPI up to ~25 feet.

OPERATION

WATCHDOG

As a safety feature, the 7I50 incorporates a watchdog circuit to disable the outputs (all outputs off) if the isolated outputs register has not been updated within a preset time interval. The outputs are also turned off in the following conditions:

1. Power UP

2. Invalid command in SPI command register (not 0xA or 0xB)

The watchdog has three timeout values selectable via on card jumpers, plus a watchdog disabled state. Timeout values are approximately 10 mS, 52 mS, and 210 mS. For normal control applications, a 10 or 52 mS timeout is suggested. ***The watchdog disable feature is for manual testing and should not be used for normal control applications.***

If the watchdog "bites", the watchdog_has_bitten (WHB) flag is set, and further updates to the output register are blocked until the WHB flag is cleared. It is recommended that host software only clear the WHB flag when it detects a watchdog timeout event. The reason for this is that if the WHB is cleared every output register update (by including a WHB = '1' bit in the output data), a watchdog timeout event might be missed.

LEDS

The 7I50 has many on card LEDS for status and debugging information. These include LEDs for power on status, watchdog status, I/O status monitoring and SPI activity

CR29 is a green LED on the lower right hand side of the card. It is illuminated when 7I50 power is on.

One LED pair, CR15 and CR17, to the left of the option jumpers, display the Watchdog_Has_Bitten status (WHB). CR15 is red and CR17 is green. If the Watchdog has bitten, CR15, the red LED will be illuminated. If the WHB status is clear, CR17, the green LED will be illuminated. Underneath CR15 and CR17 are yellow LEDs CR19 and CR20 which display the SPI CS and SPI data in signals respectively.

Each I/O pin has a monitor LED. The LEDs are yellow and are mounted in a row down the middle of the 7I50 card. These LEDS are illuminated when the corresponding I/O pin is in a low state.

When first powered up, CR15 (RED) and CR29 should be illuminated. The I/O indicator LEDS will reflect the state of the signals connected, but all output bit should be off. When running normally, CR15 (RED) should be off and CR17 and CR29 (green) should be illuminated. CR19 and CR20 may glow dimly depending on the update rate.

OPERATION

INPUT CHARACTERISTICS

All I/O pin inputs are conditioned with a 74HC14 hex Schmitt triggers. The inputs have hysteresis for improved noise immunity. Inputs are not TTL voltage compatible because of the high (~3V) threshold of the 74HC14s. Normally the internal 5V pullups will allow TTL outputs to drive the 7I50 inputs, but driving the 7I50 I/O pins with 3.3V CMOS outputs will cause unreliable operation.

OUTPUT CHARACTERISTICS

The 7I50 outputs are open drain outputs with 3.3K pull-ups to 5V. Output chips are 74LCX06 open drain hex inverters. The outputs can sink 15 mA at a 0.4V VOL. Individual outputs can sink 24 mA but no more than 3 outputs per chip may sink 24 mA at a time.

I/O POLARITY

The 7I50 is designed for use with active low sensors and actuators. This is why its default I/O state at power up or watchdog bite is all high. In addition I/O bits are inverted from the SPI data, that is a 1 bit in the SPI data will set an output bit to the low state, and a 1 bit in the input SPI data represents a low input state. The I/O monitor LEDS follow the same convention, they are illuminated when the corresponding I/O pin is in the low state.

I/O SHARING

The 7I50 has 24 I/O bits. Each bit can function as an input or an output. Each I/O bit has an active pull-down and 3.3K resistor pullup (open drain). For a I/O pin to function as an input, its output data must be set to ‘0'. The 3.3K pull-ups allow the I/O pins to be directly connected to OPTO isolators, OPT0 detectors and mechanical switches. It is suggested that the inputs not be driven high, as a programming mistake that sets the output low would cause a conflict, possibly damaging the 7I50.

LOOPBACK

The combined I/O pins allow the actual output pin states to be monitored by the SPI master if desired for error detection. Note that read data is sampled at the beginning of the SPI cycle, and outputs are updated at the end of the SPI cycle, so loopback data will reflect the previous output data.

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY (VCC)	+4.5	+5.25	VDC
5V POWER CONSUMPTION	----	150	mA
OUTPUT SINK CURRENT (@.4V Max VOL)	----	15	mA
I/0 INPUT HIGH THRESHOLD	1.8	3.3	VDC
I/0 INPUT LOW THRESHOLD	1.0	2.0	VDC
I/O VOLTAGE	-0.3	VCC	VDC
MAX TTL SHIFT RATE (2 foot cable)	----	10	MHz
MAX TTL SHIFT RATE (5 foot cable)	----	8.5	MHz
MAX DIFF SHIFT RATE (5 foot cable)	----	6	MHz
MAX DIFF SHIFT RATE (25 foot cable)	----	3	MHz
/CS –> FIRST CLOCK RISING EDGE	40	----	nS
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND