7I42/7I42TA MANUAL

FPGA I/O PROTECTOR / BREAKOUT

V1.2

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GENERAL

DESCRIPTION

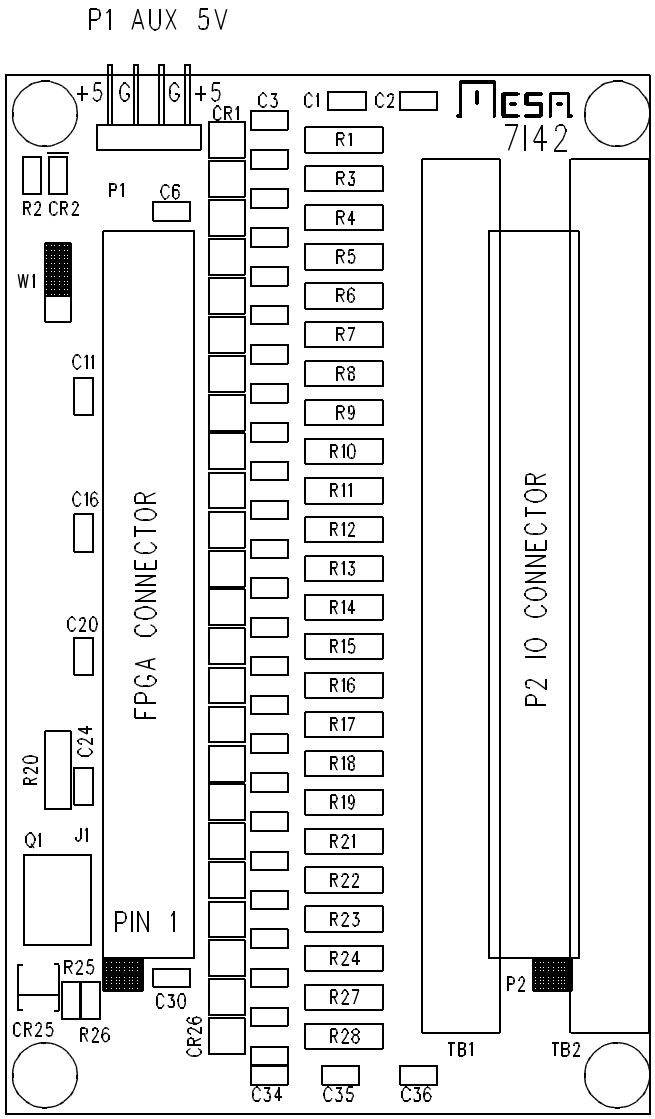
The 7I42 is a breakout card for Mesa's 50 pin I/O FPGA cards. It is available with 50 pin .1" output connector (7I42) or 3.5mm headers compatible with pluggable screw terminal blocks (7I42TA). In addition to providing a breakout function, the 7I42 protects the FPGA card from excessive input voltages and ESD. The 7I42 protects FPGA I/O from accidental contact from external voltages of +12 and -5V with built in diode clamps and 50 Ohm current limit resistors in series with all I/O pins. The 7I42 limits I/O pin bandwidth to approximately 10 MHz. Phoenix compatible 3.5 mm pluggable screw terminals are supplied with the 7I42TA

OPTION JUMPERS

The 7I42 has a single option jumper: W1. W1 determines if the 7I42 card gets its power from pin 49 of the controller connector. When W1 is in the up position (default), the 7I42 cards gets its power from pin 49. When W1 is in the down position, The 7I42 is disconnected from pin 49 and must be supplied with 5V power on P1.

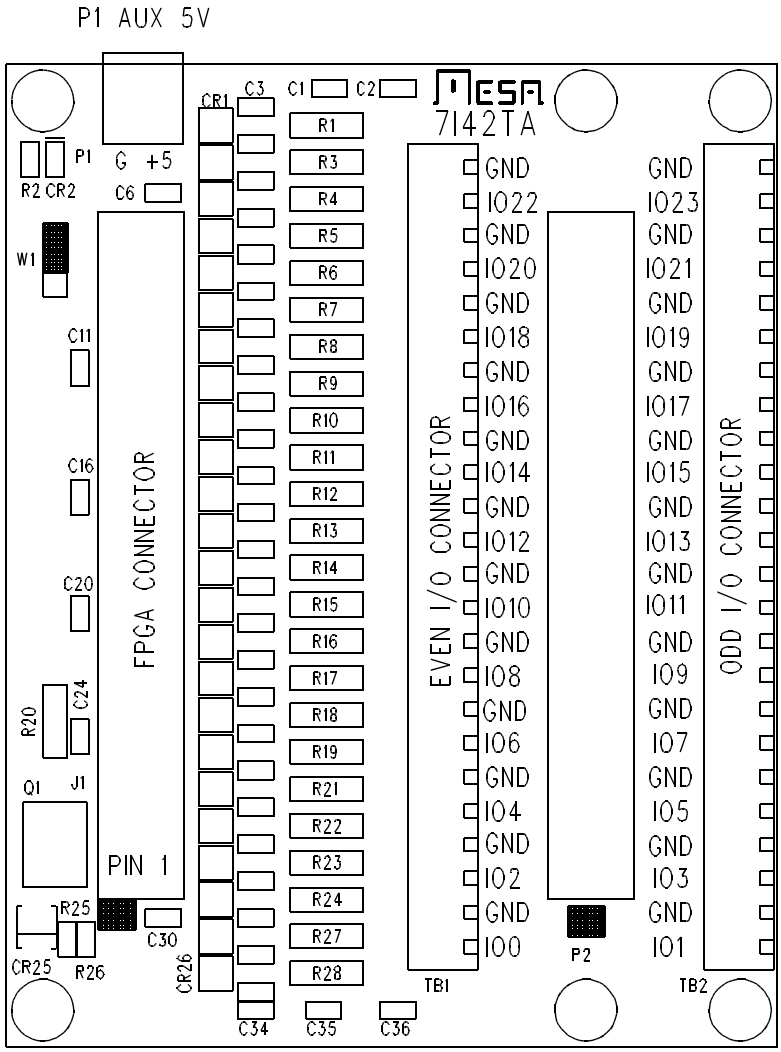
CONNECTORS

7I42 CONNECTOR LOCATIONS



CONNECTORS

7I42TA CONNECTOR LOCATIONS



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector J1 connects to the IO card that connects to the 7I42 This can be a male 50 pin header on the top of the 7I42 card or a female 50 conductor header on the bottom side of the 7I42 depending on 7I42 model.:

PIN	FUNCTION	PIN	FUNCTION
1	FPGA I/O0	25	FPGA I/O12
3	FPGA I/O1	27	FPGA I/O13
5	FPGA I/O2	29	FPGA I/O14
7	FPGA I/O3	31	FPGA I/O15
9	FPGA I/O4	33	FPGA I/O16
11	FPGA I/O5	35	FPGA I/O17
13	FPGA I/O6	37	FPGA I/O18
15	FPGA I/O7	39	FPGA I/O19
17	FPGA I/O8	41	FPGA I/O20
19	FPGA I/O9	43	FPGA I/O21
21	FPGA I/O10	45	FPGA I/O22
23	FPGA I/O11	47	FPGA I/O23
		49	+5V PWR

Note: all even pins are grounded.

AUX 5V POWER

4 pin header P1 or 2 pin terminal block P1 can be used to supply 5V power to the 7I42 if the controller cable is too long and voltage drop too high. P1 has the following pinout:

PIN	FUNCTION (7I42 REV A and earlier)	PIN	FUNCTION (7I42TA)
1	5V	1	5V (Square pad)
2	GND	2	GND
3	GND		
4	5V		

CONNECTORS

50 PIN PROTECTED I/O

The 7I42 uses 50 pin header P2 for protected I/O. The pinout is the same as J1. Header P2 pinout is as follows:

PIN	FUNCTION	PIN	FUNCTION
1	PROTECTED I/O0	25	PROTECTED I/O12
3	PROTECTED I/O1	27	PROTECTED I/O13
5	PROTECTED I/O2	29	PROTECTED I/O14
7	PROTECTED I/O3	31	PROTECTED I/O15
9	PROTECTED I/O4	33	PROTECTED I/O16
11	PROTECTED I/O5	35	PROTECTED I/O17
13	PROTECTED I/O6	37	PROTECTED I/O18
15	PROTECTED I/O7	39	PROTECTED I/O19
17	PROTECTED I/O8	41	PROTECTED I/O20
19	PROTECTED I/O9	43	PROTECTED I/O21
21	PROTECTED I/O10	45	PROTECTED I/O22
23	PROTECTED I/O11	47	PROTECTED I/O23
		49	+5V PWR

Note: all even pins are grounded

CONNECTORS

TERMINAL BLOCK PROTECTED I/O CONNECTORS

The 7I42TA uses 3.5 mm pluggable screw terminal blocks TB1 and TB2 for protected I/O. TB1 pinout is as follows:

TB1: EVEN PROTECTED I/O PINS (7I42TA only)

PIN	FUNCTION	PIN	FUNCTION
1	PROTECTED I/O0	2	GND
3	PROTECTED I/O2	4	GND
5	PROTECTED I/O4	6	GND
7	PROTECTED I/O6	8	GND
9	PROTECTED I/O8	10	GND
11	PROTECTED I/O10	12	GND
13	PROTECTED I/O12	14	GND
15	PROTECTED I/O14	16	GND
17	PROTECTED I/O16	18	GND
19	PROTECTED I/O18	20	GND
21	PROTECTED I/O20	22	GND
23	PROTECTED I/O22	24	GND

CONNECTORS

TERMINAL BLOCK PROTECTED I/O CONNECTORS

TB2: ODD PROTECTED I/O PINS (7I42TA only)

PIN	FUNCTION	PIN	FUNCTION
1	PROTECTED I/O1	2	GND
3	PROTECTED I/O3	4	GND
5	PROTECTED I/O5	6	GND
7	PROTECTED I/O7	8	GND
9	PROTECTED I/O9	10	GND
11	PROTECTED I/O11	12	GND
13	PROTECTED I/O13	14	GND
15	PROTECTED I/O15	16	GND
17	PROTECTED I/O17	18	GND
19	PROTECTED I/O19	20	GND
21	PROTECTED I/O21	22	GND
23	PROTECTED I/O23	24	GND

OPERATION

PINOUT

The 7I42 is intended to operate with FPGA I/O cards that have 24 I/O bits and IO module rack type connector pinouts (50 pin connector, all even pins grounded, +5 power on pin 49). This includes the 5I20, 5I22, 5I23, 4I34M, 4I38, 4I65, 4I69, 7I43, 7I60, 7I61, 7I62 and 3X20 cards.

I/O VOLTAGES

The 7I42 accepts 3.3V or 5V signals but will not protect 3.3V only cards from 5V inputs, as its input clamp voltage is 4.6V

DRIVE STRENGTH

The 7I42 places 50 Ohm resistors in series with each I/O pin. These resistors will limit the output drive capabilities of the attached FPGA card. When the 7I42 is used and FPGA outputs are programmed for 24 mA drive, no more than 8 mA loads should be driven if TTL output levels are to be maintained.

INPUT CLAMP

The 7I42 uses diode clamps to protect the attached FPGA card from excessive input voltage. Nominal upper clamp voltage is 4.6V and nominal lower clamp voltage is -0.7V. Maximum positive input voltage is +12V and maximum negative input voltage is -5V. Note: the 7I42 is designed to protect FPGA cards from transient and accidental connection to voltages outside of their safe I/O range. It is not designed as a input clamp for continuous overvoltages.

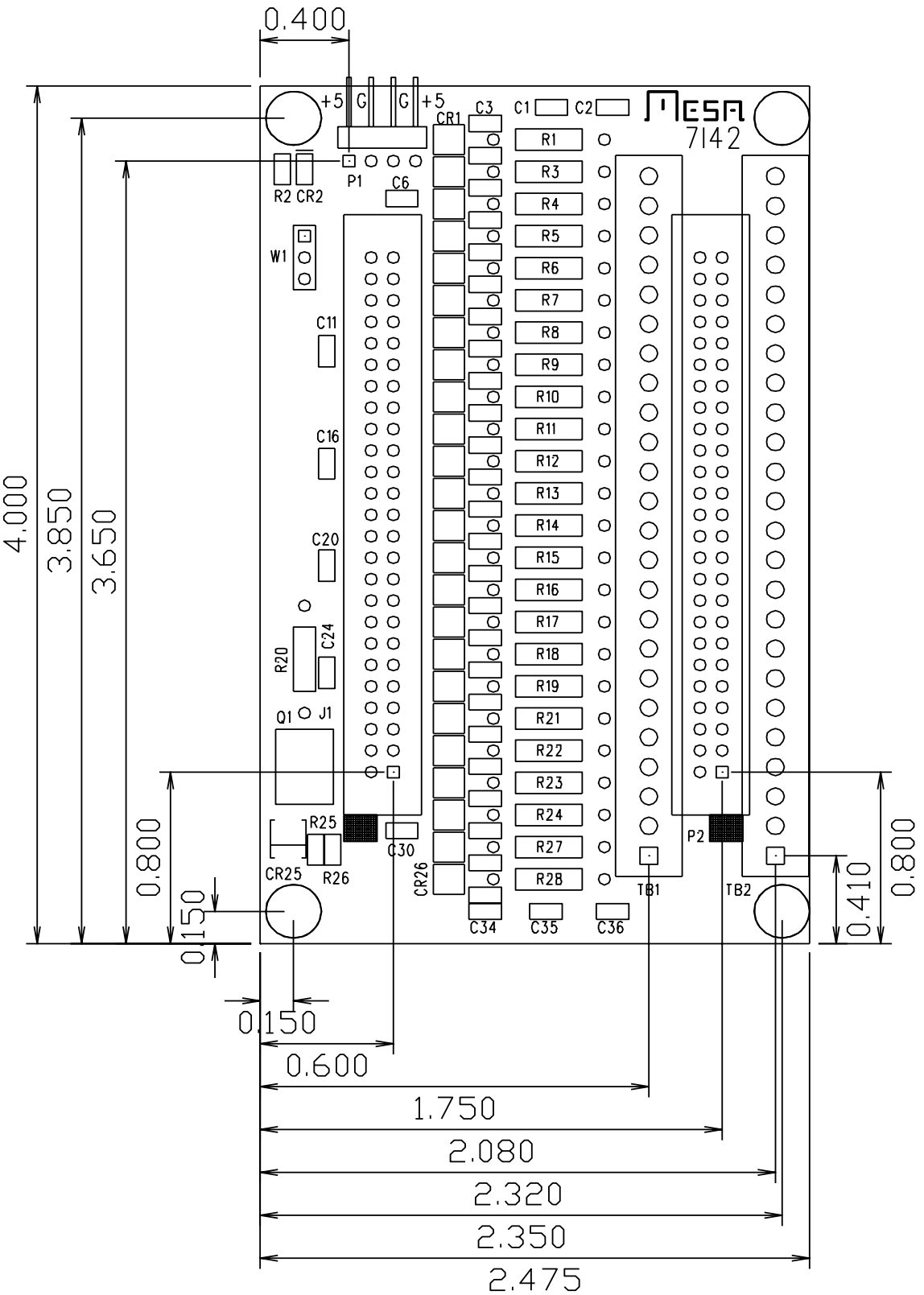
BANDWIDTH

The 7I42s 50 Ohm series resistors and parallel 220 pF capacitors limit the protected signal bandwidth to approximately 10 MHz.

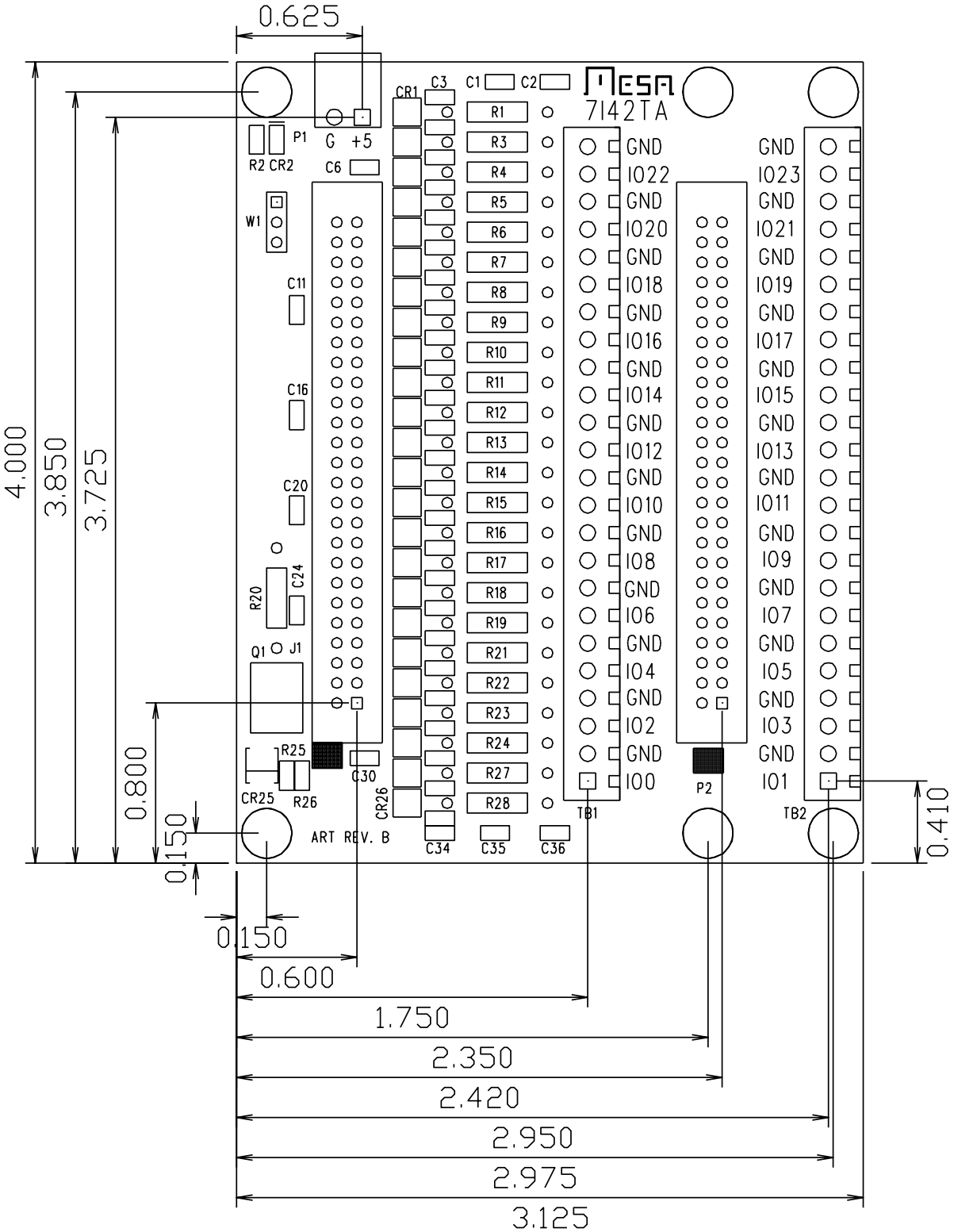
SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.5V	5.5V	VDC
5V POWER CONSUMPTION	---	50	mA
INPUT RANGE	-5	+12V	VDC
MAXIMUM NUMBER OF INPUTS	----	4	INPUTS
WITH SIMULTANEOUS 12V OVERLOAD			
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND

DRAWINGS


0.400
+5
G
G
+5
CR1
C3
C1
C2
MESA
7I42
P1
C6
R2
CR2
W1
C11
C16
C20
C24
R20
Q1
J1
R25
C30
CR25
R26
CR26
C34
C35
C36
TB1
TB2
P2
R1
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R21
R22
R23
R24
R27
R28
4.000
3.850
3.650
0.800
0.150
0.150
0.600
1.750
2.080
2.320
2.350
2.475
0.410
0.800

DRAWINGS


0.625
4.000
3.850
3.725
0.800
0.150
0.150
0.600
1.750
2.350
2.420
2.950
2.975
3.125
0.410
MESA
7I42TA
ART REV. B
TB1
TB2
P1
P2
J1
W1
Q1
GND
IO22
IO23
IO20
IO21
IO18
IO19
IO16
IO17
IO14
IO15
IO12
IO13
IO10
IO11
IO8
IO9
IO6
IO7
IO4
IO5
IO2
IO3
IO0
IO1