7C80
RPI STEP/DIR MOTION CONTROL INTERFACE

V1.4

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GENERAL

DESCRIPTION

The MESA 7C80 is step/dir oriented FPGA motion control motherboard host for a Raspberry Pi CPU. The 7C80 connects to the GPIO interface and uses SPI for FPGA communication.

The 7C80 provides 5V power for the RPI via a built in switching regulator. The 7C80 has 6 channels of differential step/dir outputs with step rate up to 10 MHz.

24 isolated inputs are provided for general control use including limit switch, control panel inputs, and up to 4 MPGs. Inputs operate with 4V to 36V DC and have 2 independent positive or negative commons for sourcing or sinking input applications. Eight 36V 2A isolated outputs allow sinking, sourcing, or combinations of both.

Spindle control includes a high speed differential or single-ended encoder input for spindle feedback and an isolated analog spindle interface with real time speed and direction control. A RS-422/RS-485 interface is provided for I/O expansion via serial I/O daughtercards or for general RS-422/RS-485 use.

In addition to the on card I/O, A FPGA expansion connector compatible with Mesa's 25 pin daughtercards or standard parallel port breakout boards allow almost unlimited I/O options including additional quadrature or absolute encoder inputs, step/dir or PWM/dir outputs, and field I/O expansion to hundreds of I/O points.

All field wiring is terminated in pluggable 3.5 mm screw terminal blocks. The 7C80 mounts in standard 107 mm DIN rail channels and is powered by 8 to 40V DC.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7C80 card is oriented in an upright position, that is, with the black P1 expansion connector on the right.

ENCODER INPUT MODE

The 7C80s high speed encoder input can be programmed for differential or single ended mode operation. W1, W2 and W3 set the encoder input mode. When W1,W2,and W3 are in the "DOWN" position, the encoder input is mode is differential. When W1,W2, and W3 are in the "UP" position, the encoder input mode is single ended or "TTL". Note that W3 controls the input mode for the ‘A’ signal, W2 controls the input mode for the ‘B’ signal and W1 controls the input mode for the index signal.

FIRMWARE MODE

Jumpers W7 and W8 are readable by the FPGA and can be used to set firmware mode options. These are currently unused and should be left in the "DOWN" position.

HARDWARE CONFIGURATION

EXPANSION CONNECTOR 5V POWER

The 7C80 has the option to supply 5V power to the breakout board connected to its expansion connector (P1).

The breakout 5V power is protected by a PTC device so will not cause damage to the 7C80 or cable if accidentally shorted. This option should only be enabled for Mesa breakout boards or boards specifically wired to accept 5V power on DB25 pins 22 through 25. When the option is disabled DB25 pins 22 through 25 are grounded. Jumper W5 controls the breakout power option.

JUMPER	POS	FUNCTION
W5	UP	5V BREAKOUT POWER ENABLED
W5	DOWN	5V BREAKOUT POWER DISABLED (*DEFAULT*)

EXPANSION CONNECTOR 5V I/O TOLERANCE

The FPGA used on the 7C80 has a 4V absolute maximum input voltage specification. To allow interfacing with 5V inputs on its expansion connector, the 7C80 has bus switches on all P1 expansion I/O pins. The bus switches work by turning off when the input voltage exceeds a preset threshold. *The 5V I/O tolerance option is the default and should normally be left enabled.*

For high speed applications where only 3.3V maximum signals are present, the 5V I/O tolerance option can be disabled. W4 controls the 5V I/O tolerance option. When W4 is on the default UP position, 5V tolerance mode is enabled. When W4 is in the DOWN position, 5V tolerance mode is disabled.

PULLUP VOLTAGE

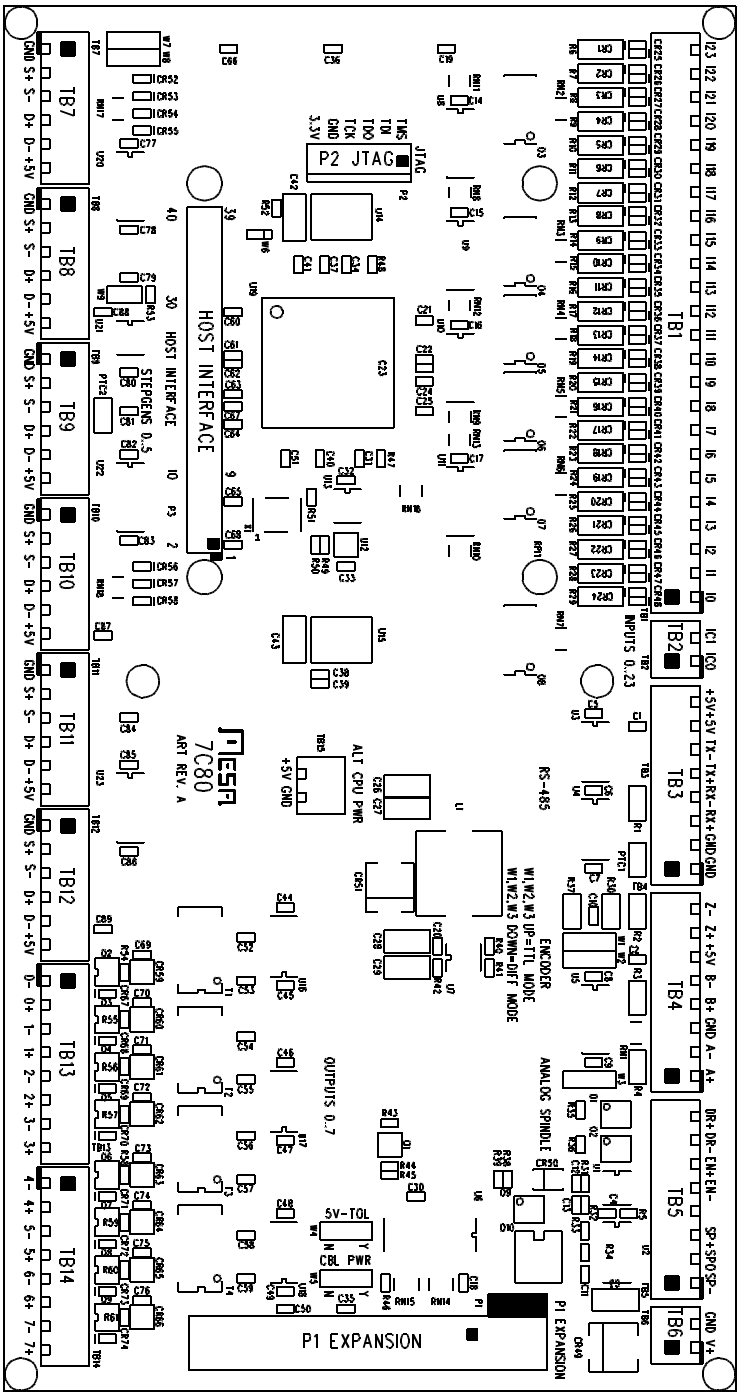
In addition to selecting the input voltage tolerance mode, Jumper W4 also selects the pull-up resistor voltage, When W4 is in the UP position the 4.7K I/O pullup resistor common is connected to 5V, When W4 is in the down position, The 4.7K I/O pullup resistor common is connected to 3.3V.

JUMPER	POS	FUNCTION
W4	UP	5V I/O TOLERANCE / 5V PULLUPS (*DEFAULT*)
W4	DOWN	NO 5V TOLERANCE / 3.3V PULLUPS

CONNECTORS

7C80 CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS

NOTE: BLACK SQUARES INDICATE PIN 1



CONNECTORS

TB6 POWER CONNECTOR PINOUT

TB6 is the 7C80s 5V power connector. TB6 is a 3.5 orange two pin 3.5 mm header with supplied plug-in screw terminal block. TB6 pinout is as follows:

PIN	FUNCTION	
1	+8V to +40V	RIGHT, SQUARE PAD
2	GND	LEFT, ROUND PAD

P2 JTAG CONNECTOR PINOUT

P2 is a JTAG programming connector. This is normally used only for debugging or if both user and fallback EEPROM configurations have been corrupted. In case of corrupted EEPROM contents the EEPROM can be re-programmed using Xilinx's Impact tool.

P2 JTAG CONNECTOR PINOUT

PIN	FUNCTION
1	TMS
2	TDI
3	TDO
4	TCK
5	GND
6	+3.3V

CONNECTORS

RPI HOST INTERFACE CONNECTOR

P3 is the connector that connects to the host CPUs GPIO connector. This connector can also supply 5V power to the CPU. A short 40 pin flat cable is used to connect the RPI to the 7C80. Maximum cable length is 2.5".

PIN	SIGNAL	USE	PIN	SIGNAL	USE
1	3.3V	NC	2	VCC	+5V
3	GPIO2/SDA1	FPGA-NU	4	VCC	+5V
5	GPIO3/SCL1	FPGA-NU	6	GND	GND
7	GPIO4	FPGA-NU	8	GPIO14/TXD0	FPGA-NU
9	GND	GND	10	GPIO15/RXD0	FPGA-NU
11	GPIO17/RTS	FPGA-NU	12	GPIO18/PCM_CLK	FPGA-NU
13	GPIO27	FPGA-NU	14	GND	GND
15	GPIO22	FPGA-NU	16	GPIO23	FPGA-NU
17	3.3V	NC	18	GPIO24	FPGA-NU
19	GPIO10/MOSI0	FPGA-SPI	20	GND	GND
21	GPIO9/MISO0	FPGA-SPI	22	GPIO25	FPGA-NU
23	GPIO11/CLK0	FPGA-SPI	24	GPIO8/CE00	FPGA-SPI
25	GND	GND	26	GPIO7/CE01	FPGA-NU
27	I2C-SD	ID EEPROM	28	ID EEPROM	FPGA-NU
29	GPIO5	FPGA-NU	30	GND	GND
31	GPIO6	FPGA-NU	32	GPIO12	FPGA-NU
33	GPIO13	FPGA-NU	34	GND	GND
35	GPIO19	FPGA-NU	36	GPIO16	FPGA-NU
37	GPIO26	FPGA-NU	38	GPIO20	FPGA-NU
39	GND	GND	40	GPIO21	FPGA-NU

Signals named FPGA-SPI are used with the standard firmwares host SPI interface. Signals named FPGA-NU are routed to the FPGA but not used by the default interface firmware. RPI 3.3V is not used on the 7C80 but the 7C80 has bypass capacitors on the RPI 3.3V pins to lower the cable AC ground impedance.

CONNECTORS

P1 EXPANSION CONNECTOR

The 7C80 has a 26 pin header to allow I/O expansion beyond the built in I/O on the 7C80 card. This I/O can include more step/dir channels, encoders, etc. This header has a pin-out that matches standard parallel port breakout cards and Mesa's 25 pin FPGA daughtercards, when terminated with a DB25 connector.

P1 PIN	DB25 PIN	P1 FUNC	P1 PIN	DB25 PIN	P1 FUNC
1	1	IO37	2	14	IO38
3	2	IO39	4	15	IO40
5	3	IO41	6	16	IO42
7	4	IO43	8	17	IO44
9	5	IO45	10	18	GND
11	6	IO46	12	19	GND
13	7	IO47	14	20	GND
15	8	IO48	16	21	GND
17	9	IO49	18	22	GND / 5V
19	10	IO50	20	23	GND / 5V
21	11	IO51	22	24	GND or 5V
23	12	IO52	24	25	GND or 5V
25	13	IO53	26	XX	GND or 5V

P1 header pins 18,20,22,24,26 (DB25 pins 22 through 25) can be tied to ground or 5V, depending on W5 position.

CONNECTORS

TB7 THROUGH TB12 STEP AND DIR CONNECTORS

Connectors TB7 through TB12 on the bottom edge of the 7C80 card are the 7C80s six step and direction connectors. Both polarities of step and direction signals are provided for differential or single ended use. TB7 through TB12 are a six pin 3.5 MM pluggable terminal blocks with supplied removable screw terminal plugs.

TB7 THROUGH TB12 CONNECTOR PINOUT

PIN	SIGNAL
1	GND
2	STEP0-
3	STEP0+
4	DIR0-
5	DIR0+
6	+5VP

Standard firmware assigns step generators in the order:

Channel 0	TB7
Channel 1	TB8
Channel 2	TB9
Channel 3	TB10
Channel 4	TB11
Channel 5	TB12

Note: 5VP pins are PTC short circuit protected 5V output pins for field wiring.

CONNECTORS

TB3 RS-422/RS-485 CONNECTOR

Connector TB3 is a high speed RS-422 or RS-485 serial interface. It also provides 5V for Mesa SSerial interface cards. TB3 is a eight pin 3.5 mm header with supplied 3.5 mm pluggable screw terminal block.

TB3 CONNECTOR PINOUT

TB3 PIN	SIGNAL
1	GND
2	GND
3	RX+
4	RX-
5	TX+
6	TX-
7	+5VP
8	+5VP

Note: 5VP pins are PTC short circuit protected 5V output pins for field wiring.

CONNECTORS

TB4 ENCODER CONNECTOR

Connectors TB4 is a high speed encoder interface. Single ended and differential encoders are supported. TB4 is a eight pin 3.5 mm header with supplied 3.5 mm pluggable screw terminal block.

TB4 CONNECTOR PINOUT

TB4 PIN	SIGNAL
1	ENCA+
2	ENCA-
3	GND
4	ENCB+
5	ENCB-
6	+5VP
7	IDX+
8	IDX-

Note: 5VP pins are PTC short circuit protected 5V output pins for field wiring.

CONNECTORS

TB1,TB2 ISOLATED INPUT CONNECTORS

Connectors TB1 and TB2 are the 7C80s isolated input connectors. TB1 is a twenty-four position 3.5 mm header supplied with four individual six pin removable screw terminal plugs. position connector with 24 inputs. TB2 has input common connections for the inputs on TB1.TB2 is a two pin 3.5 mm header with supplied pluggable screw terminal block. Inputs 0 through 7 may be used to interface to up to 4 quadrature MPGs.

TB1 CONNECTOR PINOUT

TB1 PIN	INPUT	TB1 PIN	INPUT
1	INPUT0	13	INPUT12
2	INPUT1	14	INPUT13
3	INPUT2	15	INPUT14
4	INPUT3	16	INPUT15
5	INPUT4	17	INPUT16
6	INPUT5	18	INPUT17
7	INPUT6	19	INPUT18
8	INPUT7	20	INPUT29
9	INPUT8	21	INPUT20
10	INPUT9	22	INPUT21
11	INPUT10	23	INPUT22
12	INPUT11	24	INPUT23

TB2 CONNECTOR PINOUT

1	INPUT COMMON 0 (for inputs 0 through 15)
2	INPUT COMMON 1 (for inputs 16 through 23)

CONNECTORS

TB13,TB14 ISOLATED OUTPUT CONNECTORS

Connectors TB13 and TB14 are the 7C80s isolated output connectors. TB13 and TB14 are eight pin 3.5 mm headers with supplied pluggable screw terminal blocks.

TB13 CONNECTOR PINOUT

TB13 PIN	OUTPUT
1	OUT0-
2	OUT0+
3	OUT1-
4	OUT1+
5	OUT2-
6	OUT2+
7	OUT3-
8	OUT3+

TB14 CONNECTOR PINOUT

TB14 PIN	OUTPUT
1	OUT4-
2	OUT4+
3	OUT5-
4	OUT5+
5	OUT6-
6	OUT6+
7	OUT7-
8	OUT7+

CONNECTORS

TB5 ANALOG SPINDLE INTERFACE CONNECTOR

TB5is the spindle drive interface with isolated analog output and control signals for a spindle interface.TB5 is a 8 terminal 3.5 mm header with a supplied pluggable screw terminal block.

TB5 PINOUT

TB8 PIN	SIGNAL
1	SPINDLE-
2	SPINDLE OUT
3	SPINDLE+
4	NC
5	SPINDLE ENA-
6	SPINDLE ENA+
7	SPINDLE DIR-
8	SPINDLE DIR+

OPERATION

RS-422/RS-485 INTERFACE

The 7C80 has one RS-422/RS-485 interface available on TB3. This interface is intended for I/O expansion with Mesa SSERIAL devices. The easiest way to make a cable for interfacing the 7C80 to these devices is to take a standard CAT5 or CAT6 cable, cut it in half, and wire the individual wires to the 7C80 screw terminals. The following chart gives the CAT5 to 7C80 screw terminal connections with EIA/TIA 568B colors:

TB3 PIN	SIGNAL	DIRECTION	CAT5 PIN	CAT5 568B COLOR
1	GND	FROM 7C80	4	BLUE / WHITE
2	GND	FROM 7C80	5	BLUE
3	RX+	TO 7C80	6	GREEN
4	RX-	TO 7C80	3	GREEN / WHITE
5	TX+	FROM 7C80	2	ORANGE
6	TX-	FROM 7C80	1	ORANGE / WHITE
7	+5V	FROM 7C80	7	BROWN / WHITE
8	+5V	FROM 7C80	8	BROWN

For 2 wire RS-485 applications, TX+ must be connected to RX+ and TX- must be connected to RX-.

STEP/DIR INTERFACE

The 7C80 provides six channels of step/dir interface with buffered 5V differential signal pairs. Each differential pair consists of two complementary 5V outputs. The differential signals allows reliable signal transmission in noisy environments and can directly interface with RS-422 line receivers. Step motor drives with single ended inputs connect to just one of the STEP and DIR signal outputs, that is either the STEP+/DIR+ or STEP-/DIR- signals, with the unused signals left unconnected at the 7C80. The input common signal on drives with single ended inputs connects to the 7C80s GND or 5VP pins depending on the drive type.

OPERATION

ENCODER INTERFACE

The 7C80 provides a one channel encoder interface with index. This is intended as a spindle encoder but can be used for other purposes. The encoder input can be programmed for differential or single ended encoders. The encoder interface also provides short circuit protected 5V power to the encoder. When used with single ended encoders, the ENCA+, ENCB+ and IDX+ signals are wired to the encoder and the ENCA-,ENCB-, and IDX- terminals are left unconnected.

SPINDLE INTERFACE

The 7C80 provides one analog output for spindle control. The analog output is a isolated potentiometer replacement type device. It functions like a potentiometer with SPINDLE + being one end of the potentiometer, SPINDLEOUT being the wiper and SPINDLE- being the other end. The voltage on SPINDLEOUT can be set to any voltage between SPINDLE- and SPINDLE+. Polarity and voltage range must always be observed for proper operation. The voltage supplied between SPINDLE+ and SPINDLE- must be between 5VDC an 15VDC with SPINDLE + always being more positive than SPINDLE-.

Because the analog output is isolated, bipolar output is possible, for example with SPINDLE+ connected to 5V and SPINDLE- connected to -5V, a +-5V analog output range is created. In this case the spindle output must be offset so that 50% of full scale is output when a 0V output is required.

The Spindle PWM signal is active low which means the PWM output must be inverted. This is done in the hal file with a:

setp hm2_7c80.0.pwmgen.00.out0.invert_output true

command.

SPINDLE ISOLATED OUTPUTS

The 7C80 provides 2 isolated outputs for use for spindle direction control, and spindle enable. These outputs are OPTO coupler Darlington transistors. They are all isolated from one another so can be used for pull up or pull-down individually. They will switch a maximum of 50 mA at 0 to 100 VDC. These outputs can be used for Enable/Direction or Forward/Reverse mode drives with different software setup.

OPERATION

BOARD STATUS LEDS

The 7C80 has seven LEDS for card status monitoring. The color, function and locations are as follows:

LED	COLOR	FUNCTION	OK	LOCATION
CR56	YELLOW	FPGA /INIT	OFF	BOTTOM CENTER
CR57	RED	FPGA /DONE	OFF	BOTTOM CENTER
CR58	YELLOW	LOGIC POWER	ON	BOTTOM CENTER
CR52	GREEN	USER LED3	ANY	BOTTOM LEFT
CR53	GREEN	USER LED2	ANY	BOTTOM LEFT
CR54	GREEN	USER LED1	ANY	BOTTOM LEFT
CR55	GREEN	USER LED0	ANY	BOTTOM LEFT

In normal operation CR56 and CR57 will be off. If either is on after power-up there is a problem with configuring the FPGA. CR56 is also used to signal a HostMot2 watchdog bite so will be illuminated when the LinuxCNC exits. CR58 (power LED) will also be on.

I/O STATUS LEDS

In addition to the board status LEDs, each isolated input and output has an associated yellow LED that illuminates when the input or output is active.

OPERATION

ISOLATED I/O

The 7C80 has 24 isolated inputs and 8 isolated outputs. The 24 Isolated inputs have two common pins one for inputs 0..15 and the other for inputs 16..23 . The common pins must be connected to ground for active high inputs and connected to the I/O power for active low inputs.The two independent input common pins allow interfacing to both active high and active low inputs. The 8 isolated outputs are completely floating switches so can be use for pull-up/pull-down and mixed voltage switching.

ISOLATED INPUT CHARACTERISTICS

The isolated inputs use opto-isolators with a 4.7K input series resistance. This results in an approximate current draw of 5 mA at 24V. The inputs will operate with +-4V to +-36V signals relative to input common. Isolated inputs are relatively slow and not suited for signals faster than about 5 KHz.

Inputs 0..15 use input common 0 (TB2 pin 1), while inputs 16..23 use input common 1 (TB2 pin 2)

For PNP type sensors or switches with a common positive, the input common pin is grounded and the sensor or switch applies a positive voltage to the input pin to activate the input.

For NPN type sensors or switches with a common ground, the input common is connected to +5 to +36V and the input pins are grounded to activate an input.

MPG SUPPORT

Eight of the isolated inputs can be used to support up to 4 real time quadrature MPGs. Because of the 4V input threshold, pullup resistors may be needed to interface with TTL level MPG signals.

ISOLATED OUTPUT CHARACTERISTICS

The 8 isolated outputs use full floating MOSFET switches (a DC Solid State Relay or SSR) and can be used just like a switch or relay contact. Maximum voltage is 36 VDC and maximum load current is 2A. Inductive loads must have a flyback diode. The output polarity must be observed (reversed outputs will appear to be stuck-on because of the reverse diode in the MOSFET switch).

Note: The 7C80 outputs are not short circuit protected so a current limited power supply or a 2A to 5A fuse should be used in the power source that supplies the outputs.

OPERATION

PULLUP RESISTORS

All expansion I/O pins are provided with pull-up resistors to allow connection to open drain, open collector, or OPTO devices. These resistors have a value of 4.7K so have a maximum pull-up current of ~1.07 mA (5V pull-up) or ~.7 mA (3.3V pull-up).

P1 EXPANSION CONNECTOR IO LEVELS

The Xilinx FPGAs used on the 7C80 have programmable I/O levels for interfacing with different logic families. The 7C80 does not support use of the I/O standards that require input reference voltages. All standard Mesa configurations use LVTTL levels.

Note that even though the 7C80 expansion I/O can tolerate 5V signal inputs, its outputs will not swing to 5V. The outputs are push pull CMOS that will drive to the output supply rail of 3.3V. This is sufficient for TTL compatibility but may cause problems with some types of loads. For example when driving an LED that has its anode connected to 5V, in such devices as OPTO isolators and I/O module rack SSRs, the 3.3V high level may not completely turn the LED off. To avoid this problem, either drive loads that are ground referred, Use 3.3V as the VCC for VCC referred loads, or use open drain mode.

P1 EXPANSION CONNECTOR STARTUP I/O VOLTAGE

After power-up or system reset and before the the FPGA is configured, the pull-up resistors will pull all I/O signals to a high level. If the FPGA is used for motion control or controlling devices that could present a hazard when enabled, external circuitry should be designed so that this initial state (high) results in a safe condition.

CLOCK SIGNALS

The 7C80 has a single 50 MHz clock signal from an on card crystal oscillator. The clock a can be multiplied and divided by the FPGAs clock generator block to generate a wide range of internal clock signals.

HOST INTERFACE

SPI HOST INTERFACE

GENERAL

The SPI host interface is a medium speed real time host interface with a low pin count for microcontrollers and SOC's that have built in SPI interface hardware. The 7C80s SPI interface is a slave interface and uses a SPI frame size of 32 bits for all transactions. The interface supports a SPI clock rate up to 50 MHz.

SPI MODE

The host interface uses the convention that the clock idles low, host data is shifted into the 7C80 on the SPI clock rising edge, and data is shifted out of the 7C80 on the clock falling edge. This matches SPI master setup with CPOL=0 and CPHA=0. The CS pin is active low. To support the highest transfer rates the master should have a "late sample" option.

SPI HEADER

SPI transactions always starts with a 32 bit header which contains the target register address, the read or write command, the number of data elements to be transferred and the address increment bit.

SPI HEADER

A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	C	C	C	C	I	N	N	N	N	N	N	N	X	X	X	X

The first 16 bits ("A" in the table above) are the HostMot2 register address (byte address), MSb first. The next 4 bits ("C") are the command. Currently only 2 commands are supported, read (0xA) and write (0xB). The next bit ("I") is the address increment bit. When this bit is set, the register address is incremented (by 4) after every register read/write access, allowing burst transfers from groups of sequential registers without requiring a new address to be sent. Burst transfers with the increment bit cleared can be used for multiple reads/writes to a single address for FIFO access and similar applications. The next 7 bits ("N") are the burst length for sequential transfers.Valid burst lengths are 1 through 127. The "X" bits are unused.

DATA TRANSFER SEQUENCE

For SPI reads the master sends the header followed by N frames of 32 dummy (0) bits, N being the burst length specified in the SPI header. The read data is returned on each 32 bit frame after the header frame.

On writes, the N frames of write data are sent by the master following the SPI header. The 7C80 returns dummy data when write data is being received.

HOST INTERFACE

SPI HOST INTERFACE

DATA TRANSFER SEQUENCE

Example 1: Read 3 doublewords starting at 0x1000 with increment.

Master asserts /CS	
Master sends 0x1000A830	7C80 echos dummy data
Master sends 0x00000000	7C80 echos register data @0x1000
Master sends 0x00000000	7C80 echos register data @0x1004
Master sends 0x00000000	7C80 echos register data @0x1008
Master de-asserts /CS	

Example 2: Write 4 doublewords (A,B,C,D) to location 0x600C:

Master asserts /CS	
Master sends 0x600CB040	7C80 echos dummy data
Master sends 0x0000000A	7C80 echos dummy data
Master sends 0x0000000B	7C80 echos dummy data
Master sends 0x0000000C	7C80 echos dummy data
Master sends 0x0000000D	7C80 echos dummy data
Master de-asserts /CS	

The master may de-assert /CS between frames or leave it asserted without affecting the SPI interface behavior as long as the CS idle time does not exceed the burst timeout value.

BURST TIMEOUT

Because the 7C80's SPI interface supports burst transfers of programmable length, its possible that an aborted or incorrect command could leave the 7C80 in an unknown state. To recover from this condition, the 7C80s SPI interface has a timeout on bursts. The default timeout is 50 uSec. If /CS is de-asserted for 50 usec, the SPI interface will be reset (and any pending burst aborted) so that it expects a SPI header (a new command) as the next frame. A side effect of this timeout is that a burst transfer must never de-assert /CS for longer than 50 uSec during a burst.

HOST INTERFACE

CONFIGURATION

The 7C80 is configured at power up by a SPI FLASH memory. This flash memory is an 16M bit chip that has space for two configuration files. Since all host interface logic on the 7C80 is in the FPGA, a problem with configuration means that SPI access will not be possible. For this reason there is a backup method to recover from FPGA boot failures.

FALLBACK

The backup system is called Fallback. The 7C80 flash memory normally contains two configuration file images, A user image and a fallback image. If the primary user configuration is corrupted, the FPGA will load the fallback configuration so the flash memory image can be repaired remotely without having to resort JTAG programming.

Note that if you program the 7C80 with a valid bitfile for a XC6SLX9 but not designed for a 7C80, you will likely "brick" the card. The only way a bricked card can be recovered is by using JTAG.

HOST INTERFACE

CONFIGURATION

EEPROM LAYOUT

The EEPROM used on the 7C80 for configuration storage is the M25P16. The M25P16 is a 16 M bit (2 M byte) EEPROM with 32 64K byte sectors. Configuration files are stored on sector boundaries to allow individual configuration file erasing and updating. Standard EEPROM sector layout is as follows:

0x000000	BOOT BLOCK
0x010000	FALLBACK CONFIGURATION BLOCK 0
0x020000	FALLBACK CONFIGURATION BLOCK 1
0x030000	FALLBACK CONFIGURATION BLOCK 2
0x040000	FALLBACK CONFIGURATION BLOCK 3
0x050000	FALLBACK CONFIGURATION BLOCK 4
0x060000	FALLBACK CONFIGURATION BLOCK 5
0x070000	UNUSED/FREE
0x080000	UNUSED/FREE
0x090000	UNUSED/FREE
0x0A0000	UNUSED/FREE
0x0B0000	UNUSED/FREE
0x0C0000	UNUSED/FREE
0x0D0000	UNUSED/FREE
0x0E0000	UNUSED/FREE
0x0F0000	UNUSED/FREE

HOST INTERFACE

CONFIGURATION

EEPROM LAYOUT

0x100000	USER CONFIGURATION BLOCK 0
0x110000	USER CONFIGURATION BLOCK 1
0x120000	USER CONFIGURATION BLOCK 2
0x130000	USER CONFIGURATION BLOCK 3
0x140000	USER CONFIGURATION BLOCK 4
0x150000	USER CONFIGURATION BLOCK 5
0x160000	UNUSED/FREE
0x170000	UNUSED/FREE
0x180000	UNUSED/FREE
0x190000	UNUSED/FREE
0x1A0000	UNUSED/FREE
0x1B0000	UNUSED/FREE
0x1C0000	UNUSED/FREE
0x1D0000	UNUSED/FREE
0x1E0000	UNUSED/FREE
0x1F0000	UNUSED/FREE

HOST INTERFACE

CONFIGURATION

BITFILE FORMAT

The configuration utilities expect standard FPGA bitfiles without any multiboot features enabled. If multiboot FPGA files are loaded they will likely cause a configuration failure. In addition for fallback to work, the -g next_config_register_write:disable, -g reset_on_error:enable and -g CRC:enable bitgen options must be set.

MESAFLASH

Linux utility program MESAFLASH is provided to write configuration files to the 7C80 EEPROM. These files depend on a simple SPI interface built into both the standard user FPGA bitfiles and the fallback bitfile. *The MESAFLASH utilities expect standard FPGA bitfiles without any multiboot features enabled. If multiboot FPGA files are loaded they will likely cause a configuration failure.*

If mesaflash is run with a –help command line argument it will print usage information.

The following examples assume the host SPI interface device is /dev/spidev0.0

`mesaflash --device 7C80 ––spi --addr /dev/spidev0.0  --write FPGAFILE.BIT`

Writes a standard bitfile FPGAFILE.BIT to the user area of the EEPROM.

`mesaflash --device 7C80 --spi --addr /dev/spidev0.0 --verify FPGAFILE.BIT`

Verifies the user EEPROM configuration against the bit file FPGAFILE.BIT.

`mesaflash --device 7C80 ––spi --addr /dev/spidev0.0 --fallback --write FB.BIT`

Writes the FB.BIT fallback configuration to the fallback area of the EEPROM.

HOST INTERFACE

CONFIGURATION

FREE FLASH MEMORY SPACE

Ninteen 64K byte blocks of flash memory space are free when both user and fallback configurations are installed on the 7C80. It is suggested that only the last two blocks, 0x1E0000 and 0x1F0000 in the user area, be used for FPGA application flash storage.

FALLBACK INDICATION

Mesa's supplied fallback configurations blink the red INIT LED on the (CR56 near the right side of the RPI host interface connector) if the primary configuration fails and the fallback configuration loaded successfully. If this happens it means the user configuration is corrupted or not a proper configuration for the 7C80s FPGA. This can be fixed by running the configuration utility and re-writing the user configuration**.**

FAILURE TO CONFIGURE

The 7C80 should configure its FPGA within a fraction of a second of power application. If the FPGA card fails to configure, the red /DONE LED CR57 will remain illuminated. If this happens, the 7C80s EEPROMs must be re-programmed via the JTAG connector or (faster) JTAG FPGA load followed by SPI EEPROM update.

REFERENCE INFORMATION

SPECIFICATIONS

	MIN	MAX	NOTES
GENERAL			
SUPPLY VOLTAGE	8V	40	VDC
5V CURRENT FOR HOST	----	2.5A	No ext load.
STEP/DIR OUTPUTS			
STEP/DIR OUTPUT HIGH V	4.5V	----	10 mA source
STEP/DIR OUTPUT LOW V	----	0.5V	10mA sink
STEP RATE	----	10	MHz
ISOLATED INPUTS			
INPUT RANGE	+-4V	+-36V	
INPUT RESISTANCE	4.7K	5K	
INPUT ISOLATION VOLTAGE	----	100	VDC
MAXIMUM INPUT FREQUENCY	----	5	KHz
ISOLATED OUTPUTS			
OUTPUT SWITCHED VOLTAGE	0V	+36V	
OUTPUT SWITCHED CURRENT	----	2A	
OUTPUT RESISTANCE	----	75	mOhm
OUTPUT ISOLATION VOLTAGE	----	100	VDC
MAXIMUM OUTPUT FREQUENCY	----	5	KHz

REFERENCE INFORMATION

SPECIFICATIONS

		MIN	MAX	NOTES
HIGH SPEED ENCODER INPUT				
INPUT COMMON MODE RANGE		-7	+12	Volts
INPUT TTL MODE THRESHOLD		1.4	1.8	Volts
DIFFERENTIAL MODE IMPEDANCE		118	122	Ohms
COUNT RATE		----	10 MHz	
RS-422/RS485 INTERFACE				
MAXIMUM DATA RATE		----	5	MBIT/S
INPUT COMMON MODE RANGE		-7	+12	Volts
INPUT TERMINATION RESISTOR		118	122	Ohm
OUTPUT LOW	(24 mA sink)	----	.8	Volts
OUTPUT HIGH	(24 mA source)	VCC-2	----	Volts
ANALOG SPINDLE				
SPINDLE SUPPLY VOLTAGE		5V	15V	
ISOLATED OUTPUT CURRENT		----	50	mA
ISOLATED OUTPUT VOLTAGE		0V	100	DCV
EXPANSION I/O				
OUTPUT VOLTAGE LOW		----	.4V	8 mA sink
OUTPUT VOLTAGE HIGH		2.4V	----	8 mA source
ENVIRONMENTAL				
TEMPERATURE -C VERSION		0^{o}C	70^{o}C	

REFERENCE INFORMATION

DRAWINGS