

# **4169 ANYTHING I/O MANUAL**

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# GENERAL

## DESCRIPTION

The MESA 4I69 is a general purpose programmable I/O card for the PCI bus. The 4I69 uses a XC6SLX16 or XC6SLXC25 Xilinx Spartan6 FPGA for all logic, so it is truly an Anything I/O card.

The FPGA configuration is downloadable from the PCI bus side, allowing creation of almost any kind of specialized I/O function. The 4I69 uses a bus mastering PCI bridge to give the card the ability to work with both 5V and 3.3V PCI buses and support high FPGA/PCI bus transfer rates.

Several pre-made functions are provided, including a 12 axis host based servo motor controller, a 24 channel quadrature counter, an 8 axis micro-controller based servo motor controller (SoftDMC), a simple 72 bit parallel I/O port, and a 12 channel, 32 bit timer counter card capable of running at 100 MHz. VHDL source is provided for all functions.

The 4I69 uses three 50 pin connectors with I/O module rack compatible pin-outs and interleaved grounds. Two of the connectors support s 3.3V signals. One connector supports selectable 3.3 or 2.5V signaling. All I/O signal pairs support LVDS signaling.

A 12 bit 1 MSPS A-D option with 8 inputs provides +-10V analog input capabilities. All IO can be 5V tolerant. Each connector provides 24 I/O bits for a total of 72 programmable I/O bits. A 50 Mhz crystal oscillator provides a reference clock which can be multiplied by the FPGAs DLLs for higher clock speeds.

Several I/O interface daughter cards are available for the 4I69. These cards include a 4 axis 3A Hbridge, a 2 Axis 3A stepper motor driver, an analog servo amp. interface, an RS-422/485 interface, resolver interfaces, debug LED cards and more.

# HARDWARE CONFIGURATION

## GENERAL

Hardware setup jumper positions assume that the 4I69 card is oriented in an upright position, that is, with the PC/104-PLUS connector on the top and the white PCB markings right side up.

## PC/104-PLUS SLOT NUMBER

PC104-PLUS cards have a slot number setting that corresponds to the physical PCI slots on standard PCI systems. No two I/O cards in a PC104-PLUS stack can have the same slot number. The slot numbers are assigned with jumpers W4 and W5 . The following table shows 4I69 slot numbers:

| <b>W4</b> | <b>W5</b> | <b>SLOT</b> |
|-----------|-----------|-------------|
| DOWN      | DOWN      | 0           |
| DOWN      | UP        | 1           |
| UP        | DOWN      | 2           |
| UP        | UP        | 3           |

# HARDWARE CONFIGURATION

## EEPROM ENABLE

The PLX9054 PCI-Local bus bridge chip is configured at power up via a serial EEPROM. If the EEPROM is somehow mis-programmed or corrupted, it can be impossible to re-write the EEPROM from the PC/104-PLUS bus. To avoid this problem, The EEPROM can be temporarily disabled. W3 controls the EEPROM enable function, When W2 is in the up position (default) the EEPROM is enabled. When W3 is in the down position, the EEPROM is disabled. To fix a broken EEPROM setup, you must power up the 4I69 card with the EEPROM disabled, Enable the EEPROM, and re-write the EEPROM.

## CONNECTOR POWER

The power connection on the I/O connectors can supply either 3.3V or 5V power. Supplied power should be limited to 400 mA total.

W10 selects the power supplied to P1. (The right hand I/O connector) When W6 is in the up position, 5V power is supplied to P1. When W10 is in the down position, 3.3V power is supplied to P1.

W1 selects the power supplied to P3. (The left hand I/O connector) When W1 is in the up position, 5V power is supplied to P3. When W1 is in the down position, 3.3V power is supplied to P3.

W8 selects the power supplied to P4. (The bottom I/O connector) When W8 is in the up position, 5V power is supplied to P4. When W8 is in the down position, 3.3V power is supplied to P4.

## P4 IOVCC

The IO bank that connects to P4 can have 3.3V or 2.5V power. This is intended to allow 2.5V LVDS operation on connector P4. Jumper W6 selects the IOVCC for this bank. When W6 is in the up position, 3.3V IOVCC is selected for the bank connected to P4. When W6 is in the down position, 2.5V is selected for the bank connected to P4.

# HARDWARE CONFIGURATION

## BUS SWITCH MODE

The 4I69 uses bus switch devices in series with all I/O pins. These devices allow the 4I69 inputs to be 5V tolerant and allow the I/O pins to be pulled up to 5V. The bus switch input protection function works by disconnecting the FPGA from the IO pins when the IO pin voltage rises above a preset threshold. This threshold determines the bus switch operational mode and is selectable on a per connector basis. We refer to the modes as 5V mode and 3.3V mode.

When in 5V mode, the inputs and tri-stated outputs may be pulled up to 5V. This allows driving 5V referred loads such as I/O module racks. The disadvantage of 5V mode is that the output impedance is higher in the high output state (when the FPGA pins are at 3.3V) as the bus switch is off when the FPGA pin is at 3.3V.

When 3.3V mode is selected, the bus switch is always fully on unless input voltages >4V are applied, at which point the bus switch disconnects the FPGA from the I/O pin. 3.3V mode is suggested for general use.

When the bus switch mode jumper is in the 'up' position, 5V mode is selected, when 'down', 3.3V bus switch mode is selected.

W11 Sets bus switch mode for P1, IO 0..23

W2 Sets bus switch mode for P3, IO 24..47

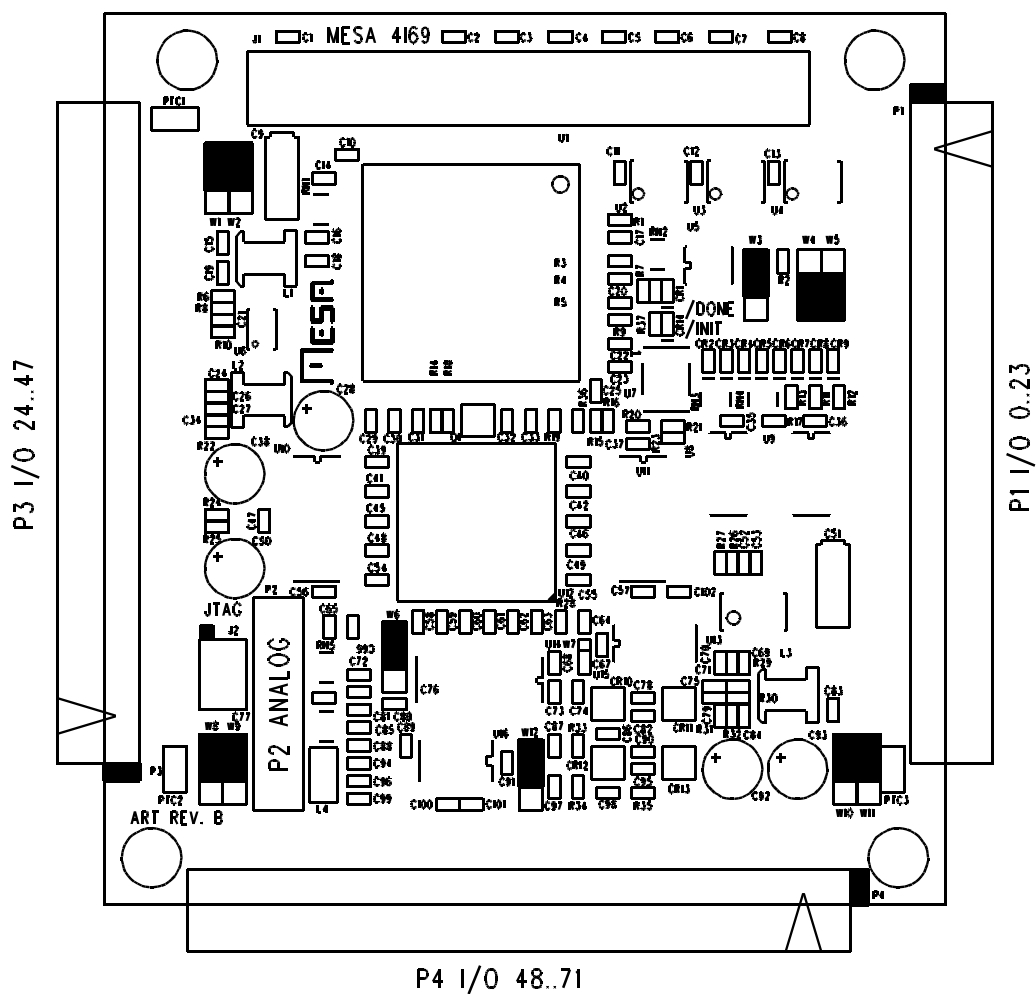
W9 Sets bus switch mode for P4, IO 48..71

## A-D INPUT MODE

If the A-D is present, jumper W12 is present and selects single ended or differential input mode. In single ended mode, the 8 input terminals are configured as 8 single ended inputs, in differential mode, the 8 terminals are configured as 4 differential input pairs. In addition to the jumper setting, the ADC chip must be programmed for the appropriate input mode.

# CONNECTORS

## CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



# CONNECTORS

## I/O CONNECTORS

P1, P3, and P4 are the 4I69's I/O connectors. These are 50 pin box headers that mate with standard 50 conductor female IDC connectors. For information on which I/O pin connects to which FPGA pin, please see the 4I69IO.PIN file on the 4I69 distribution disk. 4I69 IO connector pinouts are as follows:

### P1 CONNECTOR PINOUT

| <b>PIN</b> | <b>FUNC</b> | <b>PIN</b> | <b>FUNC</b> | <b>PIN</b> | <b>FUNC</b> | <b>PIN</b> | <b>FUNC</b> |
|------------|-------------|------------|-------------|------------|-------------|------------|-------------|
| 1          | IO0         | 2          | GND         | 3          | IO1         | 4          | GND         |
| 5          | IO2         | 6          | GND         | 7          | IO3         | 8          | GND         |
| 9          | IO4         | 10         | GND         | 11         | IO5         | 12         | GND         |
| 13         | IO6         | 14         | GND         | 15         | IO7         | 16         | GND         |
| 17         | IO8         | 18         | GND         | 19         | IO9         | 20         | GND         |
| 21         | IO10        | 22         | GND         | 23         | IO11        | 24         | GND         |
| 25         | IO12        | 26         | GND         | 27         | IO13        | 28         | GND         |
| 29         | IO14        | 30         | GND         | 31         | IO15        | 32         | GND         |
| 33         | IO16        | 34         | GND         | 35         | IO17        | 36         | GND         |
| 37         | IO18        | 38         | GND         | 39         | IO19        | 40         | GND         |
| 41         | IO20        | 42         | GND         | 43         | IO21        | 44         | GND         |
| 45         | IO22        | 46         | GND         | 47         | IO23        | 48         | GND         |
| 49         | POWER       | 50         | GND         |            |             |            |             |

# CONNECTORS

## I/O CONNECTORS

### P3 CONNECTOR PINOUT

| PIN | FUNC  | PIN | FUNC | PIN | FUNC | PIN | FUNC |
|-----|-------|-----|------|-----|------|-----|------|
| 1   | IO24  | 2   | GND  | 3   | IO25 | 4   | GND  |
| 5   | IO26  | 6   | GND  | 7   | IO27 | 8   | GND  |
| 9   | IO28  | 10  | GND  | 11  | IO29 | 12  | GND  |
| 13  | IO30  | 14  | GND  | 15  | IO31 | 16  | GND  |
| 17  | IO32  | 18  | GND  | 19  | IO33 | 20  | GND  |
| 21  | IO34  | 22  | GND  | 23  | IO35 | 24  | GND  |
| 25  | IO36  | 26  | GND  | 27  | IO37 | 28  | GND  |
| 29  | IO38  | 30  | GND  | 31  | IO39 | 32  | GND  |
| 33  | IO40  | 34  | GND  | 35  | IO41 | 36  | GND  |
| 37  | IO42  | 38  | GND  | 39  | IO43 | 40  | GND  |
| 41  | IO44  | 42  | GND  | 43  | IO45 | 44  | GND  |
| 45  | IO46  | 46  | GND  | 47  | IO47 | 48  | GND  |
| 49  | POWER | 50  | GND  |     |      |     |      |

# CONNECTORS

## I/O CONNECTORS

### P4 CONNECTOR PINOUT

| PIN | FUNC   | PIN | FUNC | PIN | FUNC   | PIN | FUNC |
|-----|--------|-----|------|-----|--------|-----|------|
| 1   | IO48/C | 2   | GND  | 3   | IO49/C | 4   | GND  |
| 5   | IO50   | 6   | GND  | 7   | IO51   | 8   | GND  |
| 9   | IO52   | 10  | GND  | 11  | IO53   | 12  | GND  |
| 13  | IO54   | 14  | GND  | 15  | IO55   | 16  | GND  |
| 17  | IO56   | 18  | GND  | 19  | IO57   | 20  | GND  |
| 21  | IO58   | 22  | GND  | 23  | IO59   | 24  | GND  |
| 25  | IO60   | 26  | GND  | 27  | IO61   | 28  | GND  |
| 29  | IO62   | 30  | GND  | 31  | IO63   | 32  | GND  |
| 33  | IO64   | 34  | GND  | 35  | IO65   | 36  | GND  |
| 37  | IO66   | 38  | GND  | 39  | IO67   | 40  | GND  |
| 41  | IO68   | 42  | GND  | 43  | IO69   | 44  | GND  |
| 45  | IO70   | 46  | GND  | 47  | IO71   | 48  | GND  |
| 49  | POWER  | 50  | GND  |     |        |     |      |

## DIFFERENTIAL PAIRS

The 4I69 supports LVDS signaling on 10 pairs of the P3 I/O connector. The pairs are marked DPx and DPx in the table above. These signals are connected to the FPGA with 100 ohm impedance differential traces on the 4I69 PCB. Note that when LVDS is used, P3's VCCIO must be set to 2.5V.

# OPERATION

## FPGA

The 4I69 use a Xilinx Spartan-III 400K gate FPGA in a 208 pin QFP package: XC3S400-PG208.

## FPGA PINOUT

The local bus and I/O interface FPGA pinouts are described in the 4I69INFC.PIN and 4I69IO.PIN files in CONFIGS directory of the distribution disk. The 4I69IO.PIN file may be used as a template for custom configurations.

## MEMORY AND I/O REGIONS

The PLX9054 PCI bridge local configuration registers can be accessed via I/O or memory. These are used to setup the PCI bridge, and for manipulating the I/O bits when configuring the FPGA.

| BAR   | MEM - I/O | WIDTH   | RANGE     |
|-------|-----------|---------|-----------|
| BAR 0 | MEMORY    | 32 BITS | 128 BYTES |
| BAR 1 | I/O       | 32 BITS | 128 BYTES |

The PLX9054 PCI bridge allows for 2 separate memory and I/O regions to be mapped to the local bus that connects to the FPGA. The default EEPROM configuration sets these up as follows:

| BAR   | ADDRESS SPACE | MEM - I/O | WIDTH   | RANGE     |
|-------|---------------|-----------|---------|-----------|
| BAR 2 | 0             | I/O       | 32 BITS | 256 BYTES |
| BAR 3 | 1             | MEMORY    | 32 BITS | 64K BYTES |

## LOCAL BUS INTERFACE

The 4I69 uses the multiplexed local bus option of the PLX9054 bridge chip to save FPGA pins. Because of the multiplexed bus, the FPGA interface logic must latch the LAD bus when ADS is active to create an internal address.

# OPERATION

## CONFIGURATION

Before the 4I69 can do anything useful it must have its FPGA configuration data downloaded from the host CPU to the FPGA on the 4I69. This is done by writing a series of bytes from the configuration file to the 4I69 card's configuration data register. Configuration data is written a byte at a time (Right justified) to any of the I/O or memory bus space regions mapped to the 4I69s local bus.

The FPGA configuration control bits must be manipulated before configuration data can be sent to the FPGA. These control bits are controlled via GPIO pins of the PLX9054 PCI bridge. The PLX9054s GPIO pins are connected to the following FPGA configuration pins:

| <b>GPIO</b> | <b>DIRECTION</b> | <b>FPGA</b> | <b>ALTERNATE</b> |
|-------------|------------------|-------------|------------------|
| GPI         | IN               | DONE        | /DACK            |
| GPO         | IN               | /PROGRAM    | /DREQ            |

Note that the DONE and /PROGRAM bits are multiplexed with DMA control lines. If these DMA control lines are needed for demand mode DMA, the DISABLECONF pin on the FPGA needs to be asserted or a /DREQ signal will reset the FPGA.

## UNUSED PINS

Due to the preferred idle local bus state on the 4I69, unused FPGA pins must be pulled up. This can be set in the 'Generate Programming File" properties box, configuration options tab, Unused IOB selection list.

## SC4I69

A utility program SC4I69.EXE is provided to send configuration files to the 4I69. The Pascal and C source for this program is available on the distribution disk, and can be used as an example for writing a custom version of download software. SC4I69 is invoked with the FPGA configuration file and the 4I69 configuration base address on the command line:

```
SC4I69 FPGAFILE.BIN
```

SC4I69 uses binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC4I69 utility sends PROM files directly to the 4I69. BIT files have their headers stripped and are bit reversed before being sent to the 4I69.



## **OPERATION**

### **CONFIGURATION**

#### **SC9054W**

Another utility SC9054W is provided for Windows 2000 and Windows XP. This utility requires the PLX9054.SYS driver and PLXAPI.DLL API SHIM to work. The source for SC9054W can be used as an example of how to access the configured 4I69 cards under Windows 2K or XP.

SC4I69 and SC9054W use binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC9054W utility sends PROM files directly to the 4I69. BIT files have their headers stripped and are bit reversed before being sent to the 4I69.

## OPERATION

### CLOCK SIGNALS

The FPGA has one on card clock source and 4 available clock inputs on I/O connector P3. The on card clock is 48 MHz routed to GCLK3. This functions as the FPGA system clock and the local bus interface clock. P3 I/O bits 56,57,58, and 59 correspond to GCLKs 7,6,5, and 4.

### LEDS

The 4I69 has 4 FPGA driven user LEDs. The user LEDs can be used for any purpose, and can be helpful as a simple debugging feature. A low output signal from the FPGA lights the LED. See the 4I69IO.PIN file for FPGA pin locations of the LED signals.

### IO LEVELS

The FPGA used on the 4I69 is a Spartan3. The Spartan3 supports many I/O standards. The 4I69 does not support use of the I/O standards that require input reference voltages, also VCCIO on the banks that connect to P1 and P2 are fixed at 3.3V so only 5 I/O options can be used on P1 and P2. The available I/O options for P1 and P2 are LVTTTL, LVCMOS\_33, LVDCI\_33, and LVDCI\_33\_DV2. P3 can use a 2.5V VCCIO which adds the following I/O standards: LVCMOS\_25, LVCMOS\_25\_DCI, LVDS\_25, LVDS\_25\_DCI, LVDSEXT\_25, LVDSEXT\_25\_DCI.

**Note that the Spartan3 chip is NOT 5V tolerant and should not have signals exceeding 3.3V applied to its inputs.**

### TERMINATION

The FPGAs used on the 4I69 support series and parallel termination that can be programmed on a pin-for-pin basis. This feature is called DCI. The 4I69 supports DCI on all I/O pins. The DCI reference resistors are all 100 Ohm 1%.

### POWER SUPPLY

The 4I69 uses on card switching regulators to supply the 3.3VCC, 2.5VAUX/VIO and 1.2VCORE core power for the FPGA. The core power supply is rated at 1 Amp. The 3.3V and 2.5V power are limited to 600 mA. All power supplies are sourced from the 5V bus power.

# SUPPLIED CONFIGURATIONS

## IOPR12

The IOPR12 configuration creates a simple 72 bit parallel I/O port. IOPR12 is a word device, all accesses read or write 16 bit words. IOPR12 creates six 12 bit ports, 2 ports per I/O connector. Each I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. For information on the register map of the IOPR12 configuration, see the regmap file in the /configs/IOPR12 directory of the 4I69 distribution disk.

## IOPR24

The IOPR24 configuration creates a simple 72 bit parallel I/O port. IOPR24 is 32 bit device, all accesses read or write 16 bit words. IOPR24 creates three 24 bit ports, one port per I/O connector.. Each I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. For information on the register map of the IOPR24 configuration, see the regmap file in the /configs/IOPR24 directory of the 4I69 distribution disk.

## 4I69LOOP

The IOPR24 configuration provides a simple way to check that all the I/O pins are OK and that most of the host interface is working. A loopback program (4I69LOOP) is provided for doing this testing. 4I69LOOP depends on an external loopback cable between I/O connectors P2, P3, and P4. 4I69LOOP perform a rotating bit test with one I/O connector programmed as outputs and the other two as inputs. All combinations of inputs and outputs are tested. In addition, a 32 bit register readback test is performed to verify 32 bit local data bus functionality.

## HOSTMOT2

The HOSTMOT2 configuration is a up to 12 channel host based servo motor or step motor controller. Host based controllers depend on the host CPU to "close" the servo loop. This has advantages and disadvantages. One advantage is that less hardware is needed, since host based software does all the math and handles all the control bits. Another advantage is that since the host based software is easily examined and modified, it is more amenable to customization and is more useful as a teaching tool.

One disadvantage is that host based motor controllers depend on fast interrupt response time, since the control loop is an interrupt driven background task. This means that host based motor controllers don't tend to work well with multitasking operating systems such as Windows or Unix. They will work with real-time operating systems or simple operating systems like DOS.

# SUPPLIED CONFIGURATIONS

## HOSTMOT2

HOSTMOT2 is available in several configurations that vary the number of servo or step generator channels, plus miscellaneous I/O options including 32 bit buffered UARTs, SPI interfaces, SSI interfaces etc.

Demonstration software provided with the 4I69 implements a PID + feedforward control loop, plus a ramp-up, slew, ramp-down, profile generator for position control applications. Demo program (newmove.exe) and sources are located in the /configs/hostmot2/support directory of the 4I69 distribution disk.

## SOFTDMC

The *SoftDMC* configuration creates a 4 or 8 axis processor based servo motor controller, with the processor embedded in the FPGA. The *SoftDMC* configuration has the advantage that the embedded processor takes care of all time critical functions, so it can control motor position and motions without host intervention.

The *SoftDMC* configuration has programmable sample and PWM rates, and can operate 4 axis at up to 50 KHz sample rate and 8 axis at up to 25 KHz sample rate.

The control loop is a PID+F loop (F=feedforward) with 16 bit tuning parameters. Position and Velocity use 32 bit parameters for wide range.

The profile generator supports position, velocity, and homing modes. Position mode includes ramp-up, slew, ramp-down motions. Velocity mode supports breakpoints and a linked list parameter loading system for accurate profiling. Profile generator uses 48 bit accumulator to allow velocities from 2 turns per day (500 line - 2000 count encoder, 4 KHz sample rate) to 60,000 RPM.

There is a separate manual available for the *SoftDMC* motion controller.

Demo programs, and tuning program (dmctune.exe) and sources are located in the /configs/softdmc/support directory of the 4I69 distribution disk.

# REFERENCE

## SPECIFICATIONS

| POWER                         | MIN    | MAX    | NOTES:                        |
|-------------------------------|--------|--------|-------------------------------|
| POWER SUPPLY                  | 4.5V   | 5.5V   |                               |
| POWER CONSUMPTION:            | ----   | 450 mA | Depends on FPGA Configuration |
| MAX 5V CURRENT TO I/O CONNS   | ---    | 500 mA | Total of all three            |
| MAX 3.3V CURRENT TO I/O CONNS | ---    | 300 mA | Total of all three            |
| TEMPERATURE RANGE -C version  | 0 °C   | +70 °C |                               |
| TEMPERATURE RANGE -I version  | -40 °C | +85 °C |                               |