# 4I24M PARALLEL PORT MANUAL

**Version 1.0**



Mesa Electronics
4175 Lakeside Drive, Suite #100
Richmond, CA 94806-1950
Tel (510) 223-9272 - Fax (510) 223-9585
E-Mail: tech@mesanet.com - Website: www.mesanet.com

# TABLE OF CONTENTS

# HANDLING PRECAUTIONS

## STATIC ELECTRICITY

The CMOS integrated circuits on the 4I24M can be damaged by exposure to electrostatic discharges. The following precautions should be taken when handling the 4I24M to prevent possible damage.

A. Leave the 4I24M in its antistatic bag until needed.

B. All work should be performed at an antistatic workstation.

C. Ground equipment into which 4I24M will be installed.

D. Ground handling personnel with conductive bracelet through 1 megohm resistor to ground.

E. Avoid wearing synthetic fabrics, particularly Nylon.

# INTRODUCTION

## GENERAL

The MESA 4I24 series of cards are 96 bit parallel I/O interfaces implemented on the PC/104 bus. The 4I24 uses 4 (4I24, 4I24I) or 3 (4I24M) socketed 82C55 PIO chips to give for a total of 96 I/O bits (4I24, 4I24I) or 72 I/O bits (4I24M). 3.3K Pullup resistors are provided on all ports to simplify interfacing to contact closure, opto-isolators, etc.

The 4I24 includes three models with different I/O connectors. The standard 4I24 uses two 50 pin headers for I/O connections. The 50 pin connectors each have 48 I/O bits, ground, and power. The 4I24I uses four 26 pin headers with ISO standard pinout (24 I/O bits per 26 pin connector, pin 2 = GND, pin 26= 5V). The 4I24M has I/O module rack compatible pinouts with three 50 pin connectors each having 24 I/O bits with interleaved grounds. 5V power on the I/O connectors is fused on the 4I24.

All 4I24 models can use the 16 bit stack through type PC/104 bus architecture. Four layer circuit card construction is used to minimize radiated EMI and provide optimum ground and power integrity. All CMOS design keeps power consumption to a minimum. The 4I24 requires only +5V for operation

The 4I24 base address is set with jumpers, and can be located anywhere in the 1024 byte I/O address space of the PC/104 bus. 4I24 cards use 16 contiguous I/O address's, but where multiple cards are used, an aliased addressing capability allows up to four 4I24 cards to share the same 10 bit base address, conserving I/O address space.

A partially loaded 48 bit version of the 4I24 and 4I24I can be provided if needed, contact MESA for availability.

# CONFIGURATION

## GENERAL

The 4I24M port address and I/O power connection options are set with jumpers. Each group of jumpers will be discussed separately by function. In the following discussions, when the words "up", "down", "right", and "left" are used it is assumed that the 4I24M I/O card is oriented with its bus connectors J1 and J2 at the bottom edge of the card (nearest the person doing the configuration).

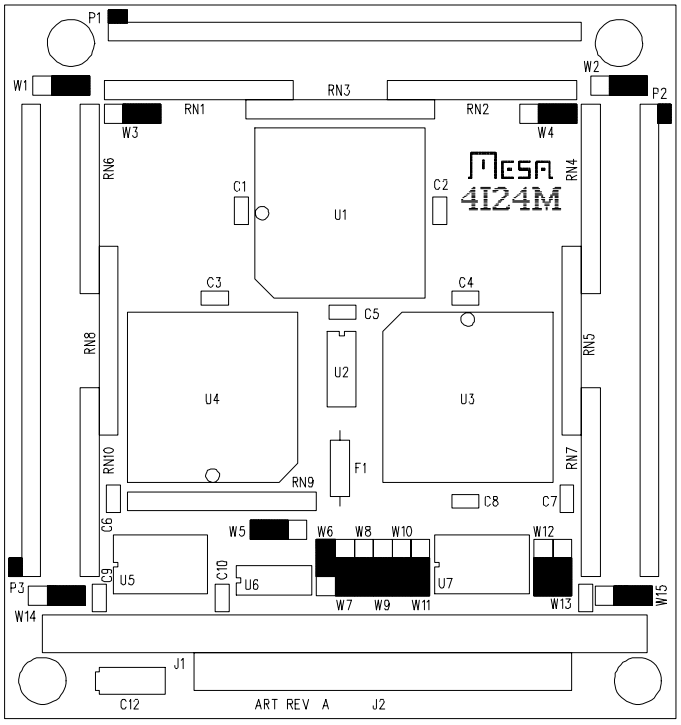
## DEFAULT JUMPER SETTINGS

Factory default 4I24M jumpering is as follows:

| FUNCTION | JUMPER(S) | SETTING |
|---|---|---|
| 4I24M power option | W5 | I/O conns pin 49 = gnd |
| 4I24M ground option | W1,W4,W15 | I/O even pins = gnd |
| 4I24M bit A0 option | W2,W3,W14 | I/O conns pin 1 = bit A0 |
| 4I24M Base address | W6,W7,W8,W9<br>W10,W11 | 0200H |
| 4I24M Aliased address | W12,W13 | 0000H |

# CONFIGURATION

## DEFAULT JUMPER SETTINGS



# CONFIGURATION

## BASE ADDRESS SELECTION

The I/O addresses of the three 82C55's on the 4I24M are selected by placing shorting jumpers on jumper blocks W6 through W11. Jumper blocks W6 through W11 have three pins and two valid shorting jumper locations, up, and down. The position of jumpers on W6 through W11 is a binary representation of the 4I24M base address. When a jumper is in the up position, it matches a high address line.

The following table shows some example base address settings

| **BASE ADDRESS** | **W6** | **W7** | **W8** | **W9** | **W10** | **W11** |
|---|---|---|---|---|---|---|
| | (A9) | (A8) | (A7) | (A6) | (A5) | (A4) |
| 0200H (Default) | up | down | down | down | down | down |
| 0290H | up | down | up | down | down | up |
| 0360H | up | up | down | up | up | down |

## ALIASED ADDRESS SELECTION

If multiple 4I24M's are used in a single system, I/O address space can be conserved by using aliased address's. Aliased addresses are an artifact caused by the partial (only 10 bit) address decoding used by most PC-bus cards. 4I24M cards actually decode A15 and A14 in addition to A0 through A9. This makes it possible to have up to four 4I24M's located at what appears to other cards in the system to be a single 16 byte block of I/O addresses. This is done by selecting the same base addresses on all cards, but selecting differing high order (aliased) addresses.

The aliased address used by a 4I24M is selected via shorting jumpers W12 and W13.

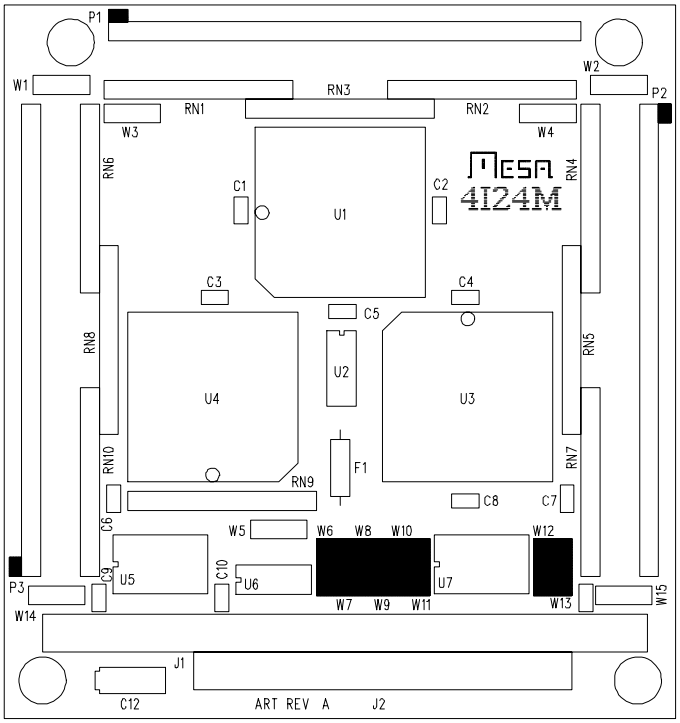
*Note that aliased addressing only makes sense when using multiple 4I24M's in a single system, and when all base address's used are the same.*

The following table shows all four of the possible aliased address settings:

| **ALIASED ADDRESS** | **W12** | **W13** |
|---|---|---|
| | (A15) | (A14) |
| BASE + 0000H (Default) | down | down |
| BASE + 4000H | down | up |
| BASE + 8000H | up | down |
| BASE + C000H | up | up |

# CONFIGURATION

## BASE AND ALIASED ADDRESS JUMPERS



# CONFIGURATION

## +5V ENABLE JUMPER

Pin 49 on all of the 4I24M I/O connectors can either be grounded or connected to system +5V through a fuse. +5V is provided on pin 49 to supply power to I/O module racks. This option is selected by the position of the shorting jumper on jumper block W5. When the jumper is in the left hand position, fused +5V power is routed to pin 49 on the I/O connectors. When W5 is in the right hand position, pin 49 is used as an additional ground. This is the default position of the +5V enable jumper.

Note that the +5V fuse is rated at 1 Amp and can be replaced without soldering. Replacement part number is LittleFuse PN 250001.

## PIN 1 OPTION JUMPERS

Pin 1 is used by some 8 and 16 I/O module racks as an additional 5V power source, but is used as an I/O bit by 24 module racks. Jumper blocks W2, W3, and W14 allow pin 1 to be connected to either +5V or the appropriate I/O bit. Jumper W3 selects the option for connector P1, jumper W2 selects the option for connector P2, and jumper W14 selects the option for connector P3.

When W2, W3, or W14 are in the left hand position, power is routed to pin 1 of the associated connector. This is the appropriate setting for most 8 and 16 module I/O racks. *Note that power to W2, W3, and W14 comes from power option jumper W5, which must be in the left hand position in order to supply power to I/O module racks*.

When W2, W3, or W14 are in the right hand position, pin 1 is an I/O bit. This is the appropriate setting for 24 module I/O racks. This is also the default position of the pin 1 option jumpers.

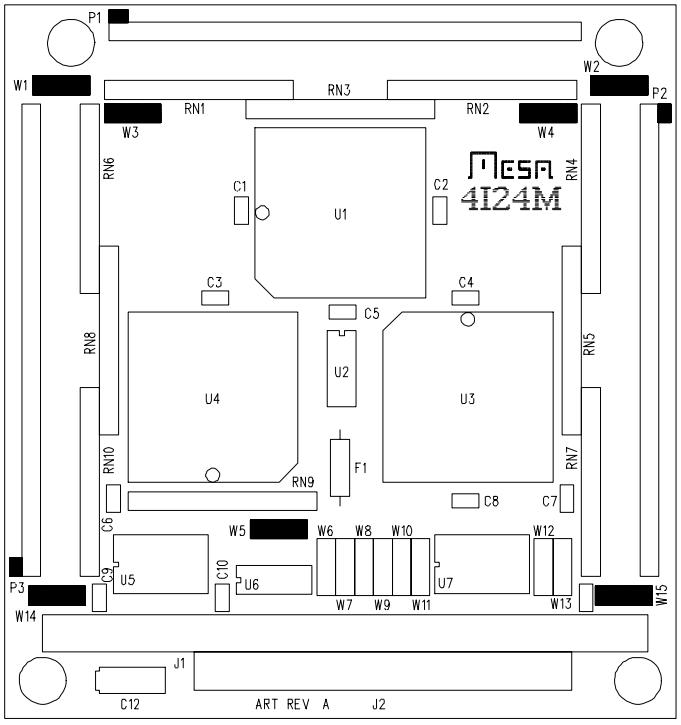
## GROUND OPTION JUMPERS

Normally all even pins of the 4I24M 50 pin I/O connectors are grounded at the 4I24M. In some circumstances, this may cause ground noise to be conducted into the system ground. All I/O ground lines can be disconnected at the 4I24M if desired.

Jumper blocks W1,W4, and W15 select whether or not the even I/O pins are grounded. Jumper W4 selects the option for connector P1, jumper W15 selects the option for connector P2, and jumper W1 selects the option for connector P3. When W1, W4, or W15 are in the left hand position, all even pins of the associated connector will be disconnected from ground. When W1, W4, or W15 are in the right hand position, all even pins of the associated connector will be grounded at the 4I24M. This is default setting of the ground option jumpers.

# CONFIGURATION

## POWER OPTION JUMPERS



# INSTALLATION

## GENERAL

When the 4I24M has been properly configured for its application, it can be inserted into a PC/104 stack. The standoffs should then be tightened to secure the 4I24M in its place. When the 4I24M is secured in the stack the 50 pin headers can be plugged in from the sides.

## I/O CONNECTOR ORIENTATION

The 50 pin connectors on the 4I24M have their pin one ends marked with a white square on the circuit card. This corresponds with the colored stripe on typical flat cable assemblies. If more positive polarization is desired, center polarized IDC header connectors should be used. These connectors will not fully mate with the pins on the 4I24M if installed backwards. A suggested center polarized 50 pin IDC header is AMP PN 1-746285-0.

# OPERATION

## PORT MAPPING

The 4I24M has three 82C55 chips. Each 82C55 chip occupies four contiguous locations in I/O space, for a total of twelve I/O locations, but the 4I24M decoding scheme actually uses sixteen I/O locations per 4I24M card, with the last four locations per card not used.

In the following table and I/O connector pinout tables the letters A, B, and C refer to individual ports on a 8255 chip (the standard 8255 port names), while the numeric suffix 0,1, or 2 refers to the specific chip.

The 82C55 ports are addressed as follows:

| ADDRESS | PORT | CONNECTOR |
|---|---|---|
| BASE +0 | A0 | P3 |
| BASE +1 | B0 | P3 |
| BASE+2 | C0 | P3 |
| BASE+3 | Control0 | |
| | | |
| BASE+4 | A1 | P1 |
| BASE +5 | B1 | P1 |
| BASE+6 | C1 | P1 |
| BASE+7 | Control1 | |
| | | |
| BASE+8 | A2 | P2 |
| BASE +9 | B2 | P2 |
| BASE+A | C2 | P2 |
| BASE+B | Control2 | |
| | | |
| BASE+C | XXX | |
| BASE +D | XXX | |
| BASE+E | XXX | |
| BASE+F | XXX | |

# OPERATION

## CONNECTOR PIN-OUT

The 4I24M 50 pin I/O connector pinouts are as follows:

### P3 CONNECTOR

| PIN | SIGNAL |
|---|---|
| 1 | A0 bit 0 or +5V fused power (W14 option) |
| 3 | A0 bit 1 |
| 5 | A0 bit 2 |
| 7 | A0 bit 3 |
| 9 | A0 bit 4 |
| 11 | A0 bit 5 |
| 13 | A0 bit 6 |
| 15 | A0 bit 7 |
| 17 | B0 bit 0 |
| 19 | B0 bit 1 |
| 21 | B0 bit 2 |
| 23 | B0 bit 3 |
| 25 | B0 bit 4 |
| 27 | B0 bit 5 |
| 29 | B0 bit 6 |
| 31 | B0 bit 7 |
| 33 | C0 bit 0 |
| 35 | C0 bit 1 |
| 37 | C0 bit 2 |
| 39 | C0 bit 3 |
| 41 | C0 bit 4 |
| 43 | C0 bit 5 |
| 45 | C0 bit 6 |
| 47 | C0 bit 7 |
| 49 | +5V fused power or GND (W5 option) |

All even pins connected to ground or open (W1 option)

# OPERATION

## P1 CONNECTOR

| PIN | SIGNAL |
|---|---|
| 1 | A1 bit 0 or +5V fused power (W3 option) |
| 3 | A1 bit 1 |
| 5 | A1 bit 2 |
| 7 | A1 bit 3 |
| 9 | A1 bit 4 |
| 11 | A1 bit 5 |
| 13 | A1 bit 6 |
| 15 | A1 bit 7 |
| 17 | B1 bit 0 |
| 19 | B1 bit 1 |
| 21 | B1 bit 2 |
| 23 | B1 bit 3 |
| 25 | B1 bit 4 |
| 27 | B1 bit 5 |
| 29 | B1 bit 6 |
| 31 | B1 bit 7 |
| 33 | C1 bit 0 |
| 35 | C1 bit 1 |
| 37 | C1 bit 2 |
| 39 | C1 bit 3 |
| 41 | C1 bit 4 |
| 43 | C1 bit 5 |
| 45 | C1 bit 6 |
| 47 | C1 bit 7 |
| 49 | +5V fused power or GND (W5 option) |

All even pins connected to ground or open (W4 option)

# OPERATION

## P2 CONNECTOR

| PIN | SIGNAL |
|---|---|
| 1 | A2 bit 0 or +5V fused power (W2 option) |
| 3 | A2 bit 1 |
| 5 | A2 bit 2 |
| 7 | A2 bit 3 |
| 9 | A2 bit 4 |
| 11 | A2 bit 5 |
| 13 | A2 bit 6 |
| 15 | A2 bit 7 |
| 17 | B2 bit 0 |
| 19 | B2 bit 1 |
| 21 | B2 bit 2 |
| 23 | B2 bit 3 |
| 25 | B2 bit 4 |
| 27 | B2 bit 5 |
| 29 | B2 bit 6 |
| 31 | B0 bit 7 |
| 33 | C2 bit 0 |
| 35 | C2 bit 1 |
| 37 | C2 bit 2 |
| 39 | C2 bit 3 |
| 41 | C2 bit 4 |
| 43 | C2 bit 5 |
| 45 | C2 bit 6 |
| 47 | C2 bit 7 |
| 49 | +5V fused power or GND (W5 option) |

All even pins connected to ground or open (W15 option)

# OPERATION

## 8255LOOP

A simple test program is supplied with the 4I24M for functional testing and verification. This program is called 8255LOOP.EXE. 8255LOOP is what's called a loopback test program. It works by sending rotating bit patterns out on all 24 bits of a 8255 programmed for all outputs, then checking to see that the same pattern has been received on a second 8255 programmed for all inputs. After this is done, 8255LOOP reverses the roles of the input and output chips and repeats the test.

The connection between the two 8255's is done with an external cable (a loopback cable!). 8255LOOP will detect most common I/O port problems including stuck bits, shorts, and opens. 8255LOOP is not very smart about major problems like incorrect port addresses, missing loopback cables etc., and will cheerfully report bit errors even if no 4I24M card is present.

To use 8255LOOP you must have a 50 conductor flat cable with female headers on each end. Because the 4I24M has three I/O connectors, you must run 8255LOOP with 2 different cable arrangements First connect P3 and P1 together with the flat cable. Make sure that the cable is properly polarized (pin1 to pin 1). Then run 8255LOOP. Next connect the loopback cable to P1 and P2, and run 8255LOOP again.

8255LOOP is invoked with 2 hexadecimal addresses on the command line. These are the addresses of the two 8255's that will be tested. If a 4I24M is set to its default (0200H) address, and has a (good) loopback cable installed, the following sequence of commands will do a fairly thorough test of the card.

(Connect loopback cable to P3 and P1)

```
8255LOOP 200 204
```

(connect loopback cable to P1 and P2)

```
8255LOOP 204 208
```

# REFERENCE INFORMATION

## SPECIFICATIONS

| | MIN | MAX | UNIT | |
|---|---|---|---|---|
| **POWER SUPPLY** | | | | |
| Voltage | 4.5 | 5.5 | V | |
| Supply current | --- | 50 | mA | (no ext. load) |
| **BUS LOADING:** | | | | |
| Input capacitance | --- | 15 | pF | |
| Input leakage current | --- | 5 | uA | |
| Output drive capability | 150 | --- | pF | |
| Output sink current | 12 | --- | mA | |
| **I/O PORT LOADING:** | | | | |
| Input logic low | -.3 | .8 | V | |
| Input logic high | 2.0 | 5.5 | V | |
| Output low | --- | .4 | V | 2.5 mA sink |
| Output high | 3.0 | --- | V | 2.5 mA source |
| **ENVIRONMENTAL:** | | | | |
| Operating temperature range | | | | |
| -I version | -40 | +85 | ºC | |
| -C version | 0 | +70 | ºC | |
| Relative humidity | 0 | 90 | Percent | |
| | | | Non-condensing | |

# REFERENCE INFORMATION

## WARRANTY

Mesa Electronics warrants the products it manufactures to be free effects in material and workmanship under normal use and service for the period of 2 years from date of purchase. This warranty shall not apply to products which have been subject to misuse, neglect, accident, or abnormal conditions of operation.

In the event of failure of a product covered by this warranty, Mesa Electronics, will repair any product returned to Mesa Electronics within 2 years of original purchase, provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may at its option, replace the product in lieu of repair.

With regard to any product returned within 2 years of purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions of operation, repairs will be billed at a nominal cost.

THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED. INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS, OR ADEQUACY FOR ANY PARTICULAR PURPOSE OR USE. MESA ELECTRONICS SHALL NOT BE LIABLE FOR ANY SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER IN CONTRACT, TORT, OR OTHERWISE.

**If any failure occurs, the following steps should be taken:**

1. Notify Mesa Electronics, giving full details of the difficulty. On receipt of this information, service data, or shipping instructions will be forwarded to you.

2. On receipt of the shipping instructions, forward the product, in its original protective packaging, transportation prepaid to Mesa Electronics. Repairs will be made at Mesa Electronics and the product returned transportation prepaid.

# REFERENCE INFORMATION

# SCHEMATICS