4I24 PARALLEL PORT MANUAL

VERSION 1.0

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HANDLING PRECAUTIONS

STATIC ELECTRICITY

The CMOS integrated circuits on the 4I24 can be damaged by exposure to electrostatic discharges. The following precautions should be taken when handling the 4I24 to prevent possible damage.

A. Leave the 4I24 in its antistatic bag until needed.

B. All work should be performed at an antistatic workstation.

C. Ground equipment into which 4I24 will be installed.

D. Ground handling personnel with conductive bracelet through 1 megohm resistor to ground.

E. Avoid wearing synthetic fabrics, particularly Nylon.

INTRODUCTION

GENERAL

The MESA 4I24 series of cards are 96 and 72 bit parallel I/O interfaces implemented on the PC/104 bus. The 4I24 uses 4 (4I24, 4I24I) or 3 (4I24M) socketed 82C55 PIO chips to give for a total of 96 I/O bits (4I24, 4I24I) or 72 I/O bits (4I24M). 3.3K Pullup resistors are provided on all ports to simplify interfacing to contact closure, opto-isolators, etc.

The 4I24 includes three models with different I/O connectors. The standard 4I24 uses two 50 pin headers for I/O connections. The 50 pin connectors each have 48 I/O bits, ground, and power. The 4I24I uses four 26 pin headers with ISO standard pinout (24 I/O bits per 26 pin connector, pin 2 = gnd, pin 26 = 5V). The 4I24M has I/O module rack compatible pinouts with three 50 pin connectors each having 24 I/O bits with interleaved grounds. 5V power on the I/O connectors is fused on the 4I24.

All 4I24 models can use the 16 bit stack through type PC/104 bus architecture. Four layer circuit card construction is used to minimize radiated EMI and provide optimum ground and power integrity. All CMOS design keeps power consumption to a minimum. The 4I24 requires only +5V for operation

The 4I24 base address is set with jumpers, and can be located anywhere in the 1024 byte I/O address space of the PC/104 bus. 4I24 cards use 16 contiguous I/O address's, but where multiple cards are used, an aliased addressing capability allows up to four 4I24 cards to share the same 10 bit base address, conserving I/O address space.

A partially loaded 48 bit version of the 4I24 and 4I24I can be provided if needed, contact MESA for availability.

CONFIGURATION

GENERAL

The 4I24 port address and I/O power connection options are set with jumpers. Each group of jumpers will be discussed separately by function. In the following discussions, when the words "up", "down", "right", and "left" are used it is assumed that the 4I24 I/O card is oriented with its bus connectors J1 and J2 at the bottom edge of the card (nearest the person doing the configuration).

DEFAULT JUMPER SETTINGS

Factory default 4I24 jumpering is as follows:
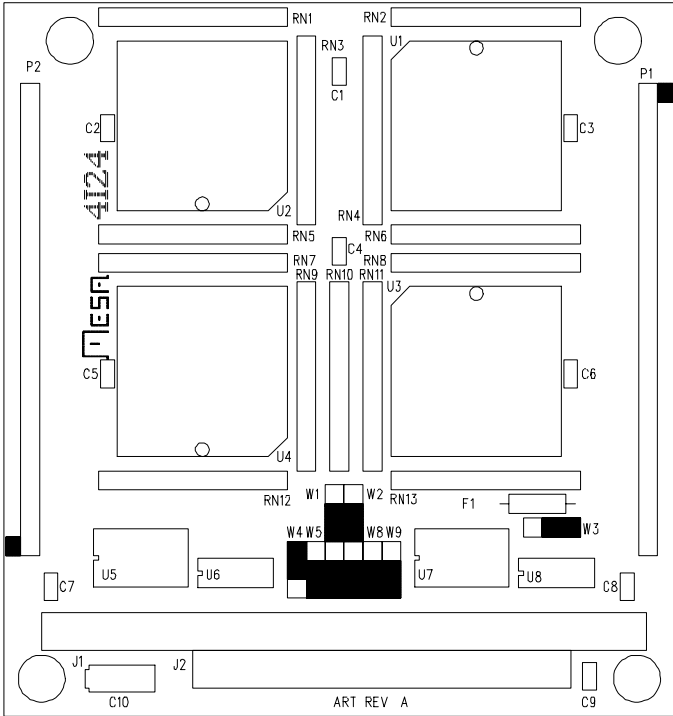
FUNCTION	JUMPER(S)	SETTING
4I24 power option	W3	I/O conns pin 50 =gnd
4I24 Base address	W4,W5,W6,W7,W8,W9	0200H
4I24 Aliased address	W1,W2	0000H

CONFIGURATION

DEFAULT JUMPER SETTINGS

CONFIGURATION

BASE ADDRESS SELECTION

The I/O addresses of the four 82C55's on the 4I24 are selected by placing shorting jumpers on jumper blocks W4 through W9. Jumper blocks W4 through W9 have three pins and two valid shorting jumper locations, up, and down. The position of jumpers on W4 through W9 is a binary representation of the 4I24 base address. When a jumper is in the up position, it matches a high address line.

The following table shows some example base address settings

BASE ADDRESS	W4	W5	W6	W7	W8	W9
	(A9)	(A8)	(A7)	(A6)	(A5)	(A4)
0200H (Default)	up	down	down	down	down	down
0290H	up	down	up	down	down	up
0360H	up	up	down	up	up	down

ALIASED ADDRESS SELECTION

If multiple 4I24's are used in a single system, I/O address space can be conserved by using aliased address's. Aliased addresses are an artifact caused by the partial (only 10 bit) address decoding used by most PC-bus cards. 4I24 cards actually decode A15 and A14 in addition to A0 through A9. This makes it possible to have up to four 4I24's located at what appears to other cards in the system to be a single 16 byte block of I/O addresses. This is done by selecting the same base addresses on all cards, but selecting differing high order (aliased) addresses.

The aliased address used by a 4I24 is selected via shorting jumpers W1 and W2.

Note that aliased addressing only makes sense when using multiple 4I24's in a single system, and when all base address's used are the same.

The following table shows all four of the possible aliased address settings:

ALIASED ADDRESS	W1	W2
	(A15)	(A14)
BASE + 0000H (Default)	down	down
BASE + 4000H	down	up
BASE + 8000H	up	down
BASE + C000H	up	up

CONFIGURATION

BASE AND ALIASED ADDRESS JUMPERS
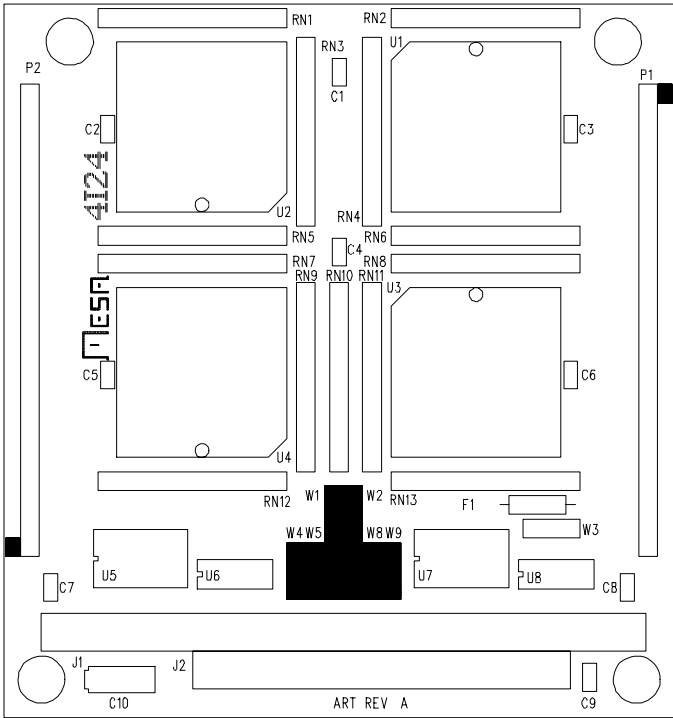
CONFIGURATION

POWER OPTION JUMPER

Pin 50 on both of the 4I24 I/O connectors can either be grounded or connected to system +5V through a fuse. This option is selected by the position of the shorting jumper on jumper block W3. When the jumper is in the left hand position, fused +5V power is routed to pin 50 on the I/O connectors. When W3 is in the right hand position, pin 50 is used as an additional ground. This is the default position.

Note that the +5V fuse is rated at 1 Amp and can be replaced without soldering. Replacement part number is LittleFuse PN 250001.

CONFIGURATION

POWER OPTION JUMPER
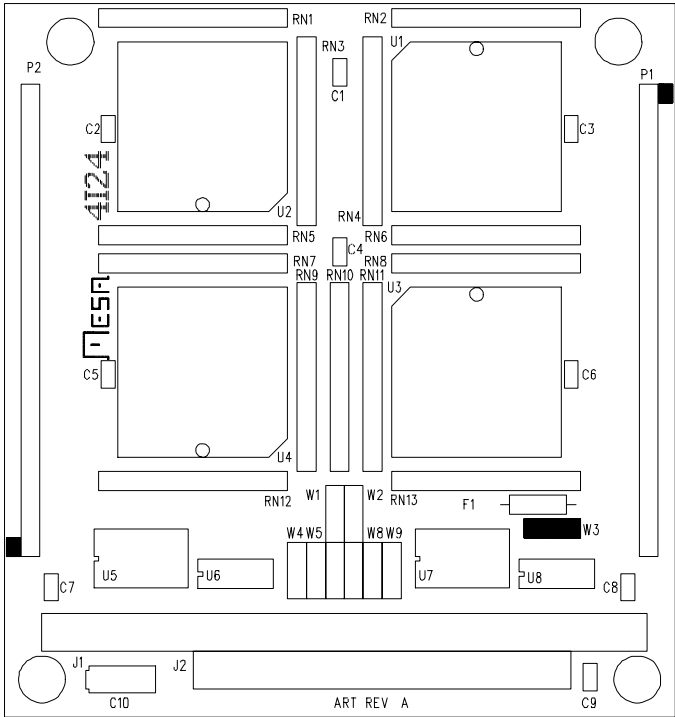
INSTALLATION

GENERAL

When the 4I24 has been properly configured for its application, it can be inserted into a PC/104 stack. The standoffs should then be tightened to secure the 4I24 in its place. When the 4I24 is secured in the stack the 50 pin headers can be plugged in from the sides.

I/O CONNECTOR ORIENTATION

The 50 pin connectors on the 4I24 have their pin one ends marked with a white square on the circuit card. This corresponds with the red stripe on typical flat cable assemblies. If more positive polarization is desired, center polarized IDC header connectors should be used. These connectors will not fully mate with the pins on the 4I24 if installed backwards. A suggested center polarized 50 pin IDC header is AMP PN 1-746285-0.

OPERATION

PORT MAPPING

The 4I24 has four 82C55 chips. Each 82C55 chip occupies four contiguous locations in I/O space, for a total of sixteen I/O locations per 4I24 card. In the following table and I/O connector pinout tables the letters A, B, and C refer to individual ports on a 8255 chip (the standard 8255 port names), while the numeric sufix 0,1,2 or 3 refers to the specific chip

The 82C55 ports are addressed as follows:

ADDRESS	PORT	CONNECTOR
BASE+0	A0	P2
BASE+1	B0	P2
BASE+2	C0	P2
BASE+3	Control0	
BASE+4	A1	P2
BASE+5	B1	P2
BASE+6	C1	P2
BASE+7	Control1	
BASE+8	A2	P1
BASE+9	B2	P1
BASE+A	C2	P1
BASE+B	Control2	
BASE+C	A3	P1
BASE+D	B3	P1
BASE+E	C3	P1
BASE+F	Control3	

OPERATION

CONNECTOR PIN-OUT

The 4I24 50 pin I/O connector pinouts are as follows:

P2 CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	A0 bit 0	2	A0 bit 1
3	A0 bit 2	4	A0 bit 3
5	A0 bit 4	6	A0 bit 5
7	A0 bit 6	8	A0 bit 7
9	B0 bit 0	10	B0 bit 1
11	B0 bit 2	12	B0 bit 3
13	B0 bit 4	14	B0 bit 5
15	B0 bit 6	16	B0 bit 7
17	C0 bit 0	18	C0 bit 1
19	C0 bit 2	20	C0 bit 3
21	C0 bit 4	22	C0 bit 5
23	C0 bit 6	24	C0 bit 7
25	A1 bit 0	26	A1 bit 1
27	A1 bit 2	28	A1 bit 3
29	A1 bit 4	30	A1 bit 5
31	A1 bit 6	32	A1 bit 7
33	B1 bit 0	34	B1 bit 1
35	B1 bit 2	36	B1 bit 3
37	B1 bit 4	38	B1 bit 5
39	B1 bit 6	40	B1 bit 7
41	C1 bit 0	42	C1 bit 1
43	C1 bit 2	44	C1 bit 3
45	C1 bit 4	46	C1 bit 5
47	C1 bit 6	48	C1 bit 7
49	Ground	50	Ground or +5V

OPERATION

P1 CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	A2 bit 0	2	A2 bit 1
3	A2 bit 2	4	A2 bit 3
5	A2 bit 4	6	A2 bit 5
7	A2 bit 6	8	A2 bit 7
9	B2 bit 0	10	B2 bit 1
11	B2 bit 2	12	B2 bit 3
13	B2 bit 4	14	B2 bit 5
15	B2 bit 6	16	B2 bit 7
17	C2 bit 0	18	C2 bit 1
19	C2 bit 2	20	C2 bit 3
21	C2 bit 4	22	C2 bit 5
23	C2 bit 6	24	C2 bit 7
25	A3 bit 0	26	A3 bit 1
27	A3 bit 2	28	A3 bit 3
29	A3 bit 4	30	A3 bit 5
31	A3 bit 6	32	A3 bit 7
33	B3 bit 0	34	B3 bit 1
35	B3 bit 2	36	B3 bit 3
37	B3 bit 4	38	B3 bit 5
39	B3 bit 6	40	B3 bit 7
41	C3 bit 0	42	C3 bit 1
43	C3 bit 2	44	C3 bit 3
45	C3 bit 4	46	C3 bit 5
47	C3 bit 6	48	C3 bit 7
49	Ground	50	Ground or +5V

OPERATION

8255LOOP

A simple test program is supplied with the 4I24 for functional testing and verification. This program is called 8255LOOP.EXE. 8255LOOP is what's called a loopback test program. It works by sending rotating bit patterns out on all 24 bits of a 8255 programmed for all outputs, then checking to see that the same pattern has been received on a second 8255 programmed for all inputs. After this is done, 8255LOOP reverses the roles of the input and output chips and repeats the test.

The connection between the two 8255's is done with an external cable (a loopback cable!). 8255LOOP will detect most common I/O port problems including stuck bits, shorts, and opens. 8255LOOP is not very smart about major problems like incorrect port addresses, missing loopback cables etc., and will cheerfully report bit errors even if no 4I24 card is present.

To use 8255LOOP you must have a 50 conductor flat cable with female headers on each end. First connect 4I24 P1 and P2 with the flat cable. Make sure that the cable is properly polarized (pin1 to pin 1). Because of the pin 1 locations of P1 and P2, the loopback cable will end up having a half twist.

8255LOOP is invoked with 2 hexadecimal addresses on the command line. These are the addresses of the two 8255's that will be tested. If a 4I24 is set to its default (0200H) address, and has a (good) loopback cable installed, the following sequence of commands will do a fairly thorough test of the card.

```
8255LOOP 200 208
8255LOOP 204 20C
```

REFERENCE INFORMATION

SPECIFICATIONS

	MIN	MAX	UNIT	
POWER SUPPLY				
Voltage	4.5	5.5	V	
Supply current	---	50	mA	(no ext. load)
BUS LOADING:				
Input capacitance	---	15	pF	
Input leakage current	---	5	uA	
Output drive capability	150	---	pF	
Output sink current	12	---	mA	
I/O PORT LOADING:				
Input logic low	-.3	.8	V	
Input logic high	2.0	5.5	V	
Output low	----	.4	V	2.5 mA sink
Output high	3.0	---	V	2.5 mA source
ENVIRONMENTAL:				
Operating temperature range				
-I version	-40	+85	ºC	
-C version	0	+70	ºC	
Relative humidity	0	90	Percent	
			Non-condensing	

REFERENCE INFORMATION

WARRANTY

Mesa Electronics warrants the products it manufactures to be free effects in material and workmanship under normal use and service for the period of 2 years from date of purchase. This warranty shall not apply to products which have been subject to misuse, neglect, accident, or abnormal conditions of operation.

In the event of failure of a product covered by this warranty, Mesa Electronics, will repair any product returned to Mesa Electronics within 2 years of original purchase, provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may at its option, replace the product in lieu of repair.

With regard to any product returned within 2 years of purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions of operation, repairs will be billed at a nominal cost.

THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED. INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS, OR ADEQUACY FOR ANY PARTICULAR PURPOSE OR USE. MESA ELECTRONICS SHALL NOT BE LIABLE FOR ANY SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER IN CONTRACT, TORT, OR OTHERWISE.

If any failure occurs, the following steps should be taken:

1. Notify Mesa Electronics, giving full details of the difficulty. On receipt of this information, service data, or shipping instructions will be forwarded to you.

2. On receipt of the shipping instructions, forward the product, in its original protective packaging, transportation prepaid to Mesa Electronics. Repairs will be made at Mesa Electronics and the product returned transportation prepaid.

REFERENCE INFORMATION

SCHEMATICS