7I65 MANUAL

8 Channel analog servo amp interface

V1.3

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GENERAL

DESCRIPTION

The 7I65 is a eight axis analog servo interface intended for operation with MESAs Anything I/O FPGA cards in motion control applications. The 7I65 has eight 16 bit DAC channels and eight TTL or differential encoder inputs. In addition the 7I65 has eight 12 bit + sign A-D inputs, eight isolated motor enable outputs and four isolated digital inputs.

Analog outputs have software selectable ranges that include -10V to +10V, -5V to +5V, 0V to +5V and 0V to +10V. Analog inputs also have software selectable ranges including -10V to +10V, -5V to +5V, -2.5V to +2.5V and 0V to +5V. Input and output ranges can be selected on a channel by channel basis.

All 7I65 Analog I/O is galvanically isolated from system logic ground to prevent ground loops and digital noise from interfering with the analog signals. A built in watchdog timer sets the analog outputs to 0V if the 7I65 has not been accessed within the settable watchdog timer interval. An on card EEPROM allows analog gain and offset values to be stored for software controlled calibration.

The 7I65 conditions the encoder input signals with input filters for TTL inputs or RS-422 receivers for differential encoder inputs. The controller connection is a 50 pin header that matches the pin-out of the 4I34M, 4I65, 4I68, 5I20, 5I22, 5I23, 5I24, 7I43 and 7I60 Anything I/O cards. 3.5 mm screw terminal compatible plugs are used for motor, analog input, and misc I/O.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I65 card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side,

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W1	ANALOG IN S/D MODE	LEFT = SINGLE ENDED
W4	CABLE/AUX POWER	DOWN = AUX
W5/W6	WATCHDOG TIMEOUT	UP/DOWN = 640 mS
W7	CH7 TTL/RS-422 SELECT	LEFT = RS-422
W8	CH5 TTL/RS-422 SELECT	LEFT = RS-422
W9	CH3 TTL/RS-422 SELECT	LEFT = RS-422
W10	CH1 TTL/RS-422 SELECT	LEFT = RS-422
W11	CH6 TTL/RS-422 SELECT	LEFT = RS-422
W12	CH4 TTL/RS-422 SELECT	LEFT = RS-422
W13	CH2 TTL/RS-422 SELECT	LEFT = RS-422
W14	CH0 TTL/RS-422 SELECT	LEFT = RS-422

ANALOG INPUT MODE

The analog inputs to the 7I65 can be single ended or differential. Jumper W1 must be set to match the desired analog input mode. For single ended mode (8 single ended channels) W1 must be in the left hand position. For differential (4 differential channels) or pseudo differential (7 pseudo-differential inputs) mode, W1 must be in the right hand position. The AD7329 A-D chip must also be programmed properly for single ended, differential or pseudo-differential mode.

HARDWARE CONFIGURATION

CABLE / AUX POWER SELECTION

The 7I65 can get its power from the controller cable or from P3, the AUX 5V power connector. Cable power is not normally sufficient to run the 7I65 and attached encoders so the default option is for AUX power. The cable power option can be used for testing the 7I65 or using the 7I65 where encoders are powered separately, not via the 7I65. W4 determines the power option. When W4 is in the "UP" position, cable power is selected. When W4 is in the down position, AUX power is selected. Note that when AUX power is selected, the 7I65 still requires cable power to enable 7I65 power-up. This is done to avoid back-powering the FPGA card from 7I65 outputs when the PC is powered down and AUX power is applied.

WATCHDOG TIMEOUT SELECTION

The 7I65 incorporates a watchdog circuit to disable the analog outputs when the host SPI interface has not updated the enable register for a selectable period of time. The timeout period is selectable via jumpers W5 and W6.

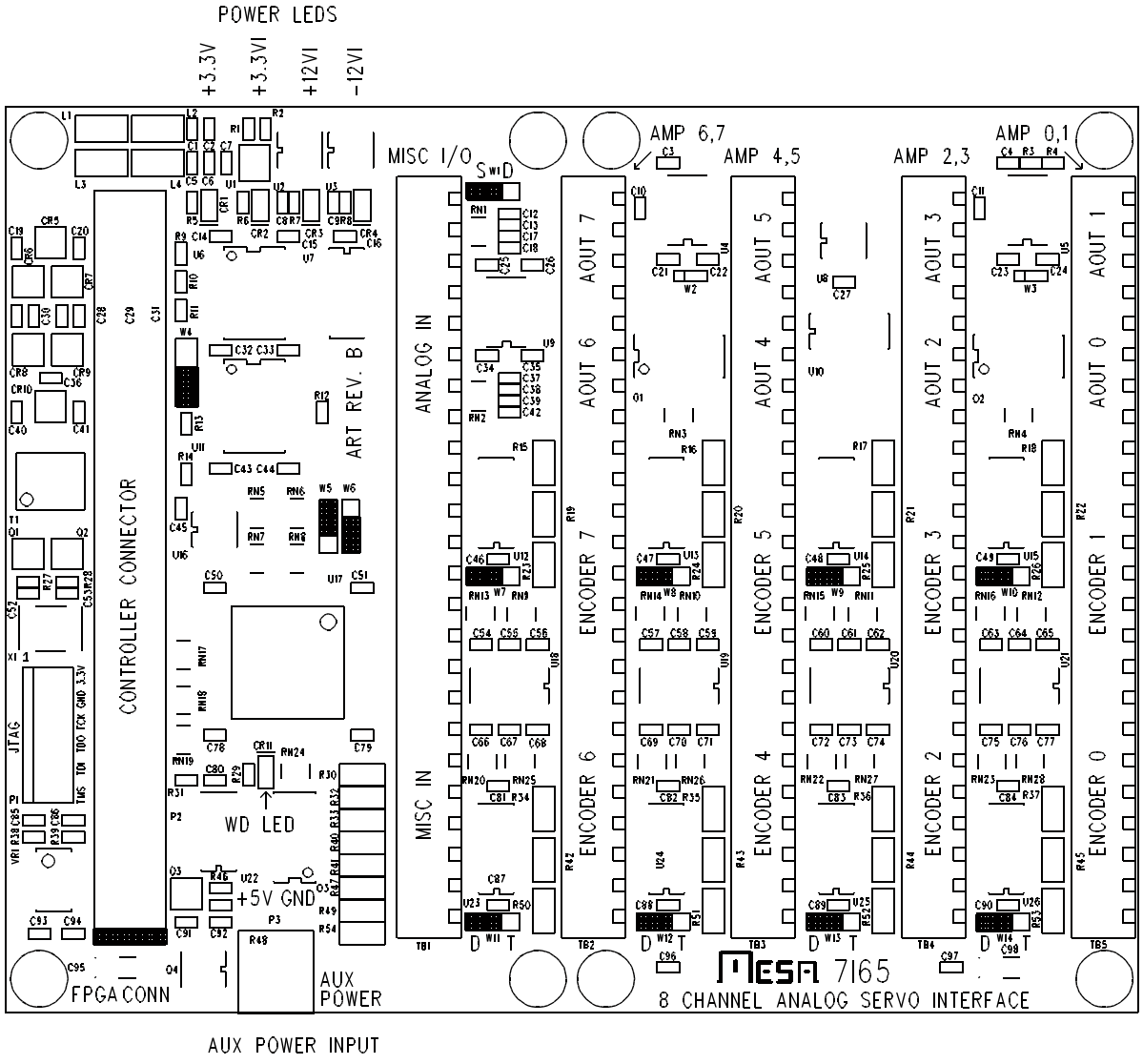
W5	W6	TIMEOUT
DOWN	DOWN	10 MS
DOWN	UP	80 MS
UP	DOWN	640 MS
UP	UP	WATCHDOG DISABLED

TTL/RS-422 ENCODER SELECTION

Each 7I65 channel has a selectable TTL or RS-422 (differential) encoder input conditioning. W7 through W14 determine the encoder input mode. When the jumpers are in the "RIGHT" position, TTL inputs are selected, When the jumpers are in the LEFT" position, RS-422 inputs are selected

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector P2 connects to the FPGA I/O card/motion controller.

PIN	FUNCTION	DIRECTION	PIN	FUNCTION	DIRECTION
1	MENCA0/1	FROM 7I65	25	ENCMUX1	TO 7I65
3	MENCB0/1	FROM 7I65	27	ENCMUX0	TO 7I65
5	MIDX0/1	FROM 7I65	29	/SPIFRAME	TO 7I65
7	MENCA2/3	FROM 7I65	31	SPIDI	TO 7I65
9	MENCB2/3	FROM 7I65	33	SPCLK	TO 7I65
11	MIDX2/3	FROM 7I65	35	SPIDO	FROM 7I65
13	MENCA4/5	FROM 7I65	37	CS2	TO 7I65
15	MENCB4/5	FROM 7I65	39	CS1	TO 7I65
17	MIDX4/5	FROM 7I65	41	CS0	TO 7I65
19	MENCA6/7	FROM 7I65	43	/LDAC	TO 7I65
21	MENCB6/7	FROM 7I65	45	/ENABLE	TO 7I65
23	MIDX6/7	FROM 7I65	47	RESET	TO 7I65
			49	+5V PWR	TO 7I65

Note: all even pins are grounded.

AUX 5V POWER

2 pin 3.5 mm connector P3 is normally used to supply 5V power to the 7I65. P3 has the following pinout:

PIN	FUNCTION
1	5V (SQUARE PAD)
2	GND

CONNECTORS

TERMINAL BLOCK SERVO AMP/ENCODER CONNECTORS

The 7I65 servo amplifier / encoder connectors (TB2 through TB5) are 3.5MM 24 pin headers with mating pluggable screw terminal blocks included.

TB5 PIN	FUNCTION	DIR	TB4 PIN	FUNCTION	DIR
1	ENCA0	TO 7I65	1	ENCA2	TO 7I65
2	/ENCA0	TO 7I65	2	/ENCA2	TO 7I65
3	GND	FROM 7I65	3	GND	FROM 7I65
4	ENCB0	TO 7I65	4	ENCB2	TO 7I65
5	/ENCB0	TO 7I65	5	/ENCB2	TO 7I65
6	+5V	FROM 7I65	6	+5V	FROM 7I65
7	IDX0	TO 7I65	7	IDX2	TO 7I65
8	/IDX0	TO 7I65	8	/IDX2	TO 7I65
9	ENCA1	TO 7I65	9	ENCB3	TO 7I65
10	/ENCA1	TO 7I65	10	/ENCA3	TO 7I65
11	GND	FROM 7I65	11	GND	FROM 7I65
12	ENCB1	TO 7I65	12	ENCB3	TO 7I65
13	/ENCB1	TO 7I65	13	/ENCA3	TO 7I65
14	+5V	FROM 7I65	14	+5V	FROM 7I65
15	IDX1	TO 7I65	15	IDX3	TO 7I65
16	/IDX1	TO 7I65	16	/IDX3	TO 7I65
17	ENABLE0-	FROM 7I65	17	ENABLE2-	FROM 7I65
18	ENABLE0+	FROM 7I65	18	ENABLE2+	FROM 7I65
19	AGND	FROM 7I65	19	AGND	FROM 7I65
20	AOUT0	FROM 7I65	20	AOUT2	FROM 7I65
21	ENABLE1-	FROM 7I65	21	ENABLE3-	FROM 7I65
22	ENABLE1+	FROM 7I65	22	ENABLE3+	FROM 7I65
23	AGND	FROM 7I65	23	AGND	FROM 7I65
24	AOUT1	FROM 7I65	24	AOUT3	FROM 7I65

CONNECTORS

TERMINAL BLOCK SERVO AMP/ENCODER CONNECTORS

TB3 PIN	FUNCTION	DIR	TB2 PIN	FUNCTION	DIR
1	ENCA4	TO 7I65	1	ENCA6	TO 7I65
2	/ENCA4	TO 7I65	2	/ENCA6	TO 7I65
3	GND	FROM 7I65	3	GND	FROM 7I65
4	ENCB4	TO 7I65	4	ENCB6	TO 7I65
5	/ENCB4	TO 7I65	5	/ENCB6	TO 7I65
6	+5V	FROM 7I65	6	+5V	FROM 7I65
7	IDX4	TO 7I65	7	IDX6	TO 7I65
8	/IDX4	TO 7I65	8	/IDX6	TO 7I65
9	ENCA5	TO 7I65	9	ENCB7	TO 7I65
10	/ENCA5	TO 7I65	10	/ENCA7	TO 7I65
11	GND	FROM 7I65	11	GND	FROM 7I65
12	ENCB5	TO 7I65	12	ENCB7	TO 7I65
13	/ENCB5	TO 7I65	13	/ENCA7	TO 7I65
14	+5V	FROM 7I65	14	+5V	FROM 7I65
15	IDX5	TO 7I65	15	IDX7	TO 7I65
16	/IDX5	TO 7I65	16	/IDX7	TO 7I65
17	ENABLE4-	FROM 7I65	17	ENABLE6-	FROM 7I65
18	ENABLE4+	FROM 7I65	18	ENABLE6+	FROM 7I65
19	AGND	FROM 7I65	19	AGND	FROM 7I65
20	AOUT4	FROM 7I65	20	AOUT6	FROM 7I65
21	ENABLE5-	FROM 7I65	21	ENABLE7-	FROM 7I65
22	ENABLE5+	FROM 7I65	22	ENABLE7+	FROM 7I65
23	AGND	FROM 7I65	23	AGND	FROM 7I65
24	AOUT5	FROM 7I65	24	AOUT7	FROM 7I65

CONNECTORS

TERMINAL BLOCK ANALOG IN / MISC IN CONNECTOR

The 7I65 Analog input / miscellaneous input connector is a 3.5 mm pluggable screw terminal (TB1) with 24 connections. TB1 pinout is as follows

TB1 PIN	FUNCTION	DIR
1	MISCIN0+	TO 7I65
2	MISCIN0-	TO 7I65
3	MISCIN1+	TO 7I65
4	MISCIN1-	TO 7I65
5	MISCIN2+	TO 7I65
6	MISCIN2-	TO 7I65
7	MISCIN3+	TO 7I65
8	MISCIN3-	TO 7I65
9	AGND	FROM 7I65
10	+3.3VI	FROM 7I65
11	+12VI	FROM 7I65
12	-12VI	FROM 7I65
13	AGND	FROM 7I65
14	AGND	FROM 7I65
15	AIN0/DIFF0+	TO 7I65
16	AIN1/DIFF0-	TO 7I65
17	AIN2/DIFF1+	TO 7I65
18	AIN3/DIFF1-	TO 7I65
19	AGND	FROM 7I65
20	AIN4/DIFF2+	TO 7I65
21	AIN5/DIFF2-	TO 7I65
22	AIN6/DIFF3+	TO 7I65
23	AIN7/DIFF4-/PDIF-	TO 7I65
24	AGND	FROM 7I65

OPERATION

ENCODER INPUT CIRCUIT

The 7I65 input circuit is different depending on whether TTL or RS-422 encoder types have been selected.

In TTL mode the input circuit on the encoder A,B, and index inputs consists of a RC filter followed by a Schmitt trigger. This helps to reject spike noise on the encoder lines. The input circuit inverts the signals, so, for example, an active high index signal will be active low at the controller interface.

In RS-422 mode, the input consists of a 132 Ohm termination resistor and a 26LS32 RS-422 differential receiver.

MAXIMUM COUNT RATE

In TTL mode, the input RC filter limits the maximum encoder input frequency to approximately 1 MHz. This corresponds to 4 million counts per second with most quadrature counters (4X mode and encoder filtering off)). The maximum input frequency may be lower with encoders that have high value (>1K Ohm) pull-up resistors on open collector outputs.

In RS-422 mode, maximum encoder input frequency limited by the 7I65s encoder multiplexing. Default multiplexing rate with HostMot2 firmware is ClockLow/8, approximately 4 an 6 MHz, giving a maximum resolvable input frequency of 2 to 3 MHz.

In both TTL and RS-422 modes, encoder count rate is further limited by HostMot2s input filtering to ~5 to ~8 million counts per second (encoder filtering off) and ~1 to ~1.6 million counts per second (encoder filtering on). Multiplexing rate can be increased if desired but high multiplex rates will require short cables between the FPGA controller card and the 7I65 due to signal integrity and time-of-flight considerations. The 7I65s CPLD can also be modified to allow mix of multiplexed and un-multiplexed encoder inputs for applications that require extremely high encoder count rates (> 8MHz) on some inputs.

ANALOG OUTPUTS

The 7I65 has eight analog outputs with 16 bit resolution. Two AD5754 quad DAC chips are used to generate the analog outputs. Each analog output channel has software selectable output ranges, ranges include -10V to +10V, -5V to +5V, 0 to +10V and 0 to +5V. The analog outputs are forced to 0V at power up and when the watchdog "bites". Analog output update can be done either at the end of the SPI frame or simultaneously by strobing the /LDAC pin. Individual 7I65 analog outputs can drive low impedance loads of down to 1K Ohms (10 mA at ±10V) but total analog output current is limited to 24 mA. Analog outputs are isolated from digital ground but all eight channels share a common analog ground signal (AGND). This ground signal is also common with the analog inputs.

OPERATION

ENABLE OUTPUTS

Each 7I65 channel has an isolated enable output intended to drive the enable input on the servo amplifier. Each enable output is a OPTO-Coupler NPN transistor switch. The ENABLE+ lead is the transistor collector and the ENABLE- lead is the transistor emitter. The switches can drive active low and active high Amplifier enables. Each enable output is rated 5mA max at 30V.

ANALOG INPUTS

The 7I65 has a eight analog input channels. These inputs connect to a 12 bit plus sign A-D converter (AD7329) with ±10 V, ±5 V, ±2.5 V, 0 to +10V input ranges. Either eight single ended input channels or four full differential inputs can be configured. The analog inputs use the same isolated analog ground as the analog outputs. For differential inputs, input pairs are even and odd AIN signals. For example differential pair 0 is AIN0 (+) and AIN1 (-).

MISC INPUTS

Four isolated digital inputs are provided by the 7I65. These OPTO-Isolated inputs accept DC input voltages from 4 to 24VDC. They are read at the same time as the enable outputs are updated.

ISOLATED POWER

A small amount of isolated power is available on terminal block TB1. This can be used for analog input conditioning circuitry or other applications that need to maintain the isolated nature of the ANALOG I/O. +12, -12 and 3.3V are available. Maximum current draw from ±12 is 5 mA. Maximum draw from 3.3V is 50 mA.

CONTROLLER CABLE LENGTH

Suggested maximum controller cable length is 5 feet. Longer cables are possible but SPI and encoder multiplex timing may need to be changed to accommodate the signal delays. Each foot of flat cable adds ~1.5 nS of one way delay but adds ~3 nS skew to the mutiplexed encoder data and the SPI readback data. This skew will limit clock rates of SPI reads and encoder multiplexing rate, but will not effect SPI write timing.

5V POWER

The 7I65 requires ~250 mA of 5V power for operation. Encoder power can also be supplied from the 7I65's 5V source. Power for the 7I65 is normally supplied from AUX power connector P3, but can be supplied via pin 49 of the 50 conductor controller cable, if encoders will be powered from a source other than the 7I65s 5V encoder power pins.

OPERATION

SPI INTERFACE

All Analog I/O, enable outputs, misc inputs and EEPROM access on the 7I65 card are done via SPI. The 7I65s SPI interface includes the normal SPIDI, SPIDO, SPIClk, and SPIFrame signals along with CS0, CS1 and CS2. The following table show the SPI device decoding:

SELECT	CS2	CS1	CS0	DEVICE
0	0	0	0	SPIDI -> SPIDO Loopback through isolation
1	0	0	1	AD5754 DAC (Analog out channels 0..3)
2	0	1	0	AD5754 DAC (Analog out channels 4..7)
3	0	1	1	AD7329 ADC (Analog in channels 0..7)
4	1	0	0	CPLD (Enable out and Misc in)
5	1	0	1	Unused
6	1	1	0	Unused
7	1	1	1	M25P10 EEPROM

SPI SETTINGS

The different SPI devices on the 7I65 have different timing requirements. These requirements are determined by the SPI chip characteristics, signal delays inherent in the signal isolation, and cable delays and dispersion. The following table gives SPI settings for each of the devices on the 7I65 card, assuming a 5 foot maximum controller cable length. Note that SPI readback speed limits ADC shift clock due to signal skew across the isolation and CPLD and EEPROM readback speed due to cable delays. These clock rates will be improved when the FPGA SPI interface incorporates read data skew adjust.

DEVICE	PN	MAX CLOCK	CPOL	CPHA	BITS
DAC	AD5754	25 MHz	1	0	24
ADC	AD7329	6 MHz	1	0	16
CPLD	XC95144	8 MHz	1	0	12
EEPROM	M25P10	8 MHz	1	1	VARIABLE

OPERATION

SPI SETTINGS

The example programs BSPI FPGA SPI channel descriptor initialization demonstrates basic SPI channel setup. Detailed data formatting and option setup command for the DACs, ADC, and EEPROM are beyond the scope of this manual. For this information, the manufacturers data sheets should be consulted. The AD7329 and AD5754 chips are manufactured by Analog Devices (www.analog.com). The EEPROM is manufactured by STMicro (www.st.com).

ENABLE OUT AND MISC INPUT SPI DEVICE

The writing of the eight enable outputs and reading of the four miscellaneous inputs is done via access to a CPLD SPI device on the 7I65 card. This SPI device uses 12 bit frames with the following format:

SEND DATA

B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
C3	C2	C1	C0	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0

RECEIVE DATA

B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
C3	C2	C1	WDB	XX	XX	XX	XX	MI3	MI2	MI1	MI0

The first nibble (C3..C0) is the command. Valid commands are 0xA (Write) and 0xB (Read). Write commands do three things:

1. Update the Enable bits (ENA0.. ENA7)

2. Echo the Misc In and status bits (MI0..MI3)

3. Reset the watchdog

The enable outputs switches are on when the corresponding ENA bit is high.

Read commands only do #2, echo the Misc In and status bits. The receive data is identical for read and write commands. The first three bits echo the 3 most significant command bits. Bit 8 (WDB) indicates that the watchdog has bitten (active high). Bits 4 through 7 are currently unused. The least significant 4 bits echo the status of the Misc Input bits (High indicates high input status).

OPERATION

WATCHDOG

As a safety feature, the 7I65 incorporates a watchdog circuit to disable the analog outputs (all outputs set to 0V) and disable all enable outputs if the enable register has not been updated within a preset time interval. The analog outputs are also cleared in these conditions:

1. Power UP

2. Power Down

3. Invalid command in Enable Register (not 0xA or 0xB)

4. External Enable high

5. External Reset High

The watchdog has three timeout values selectable via on card jumpers, plus a watchdog disabled state. Timeout values are approximately 10 mS, 80 mS, and 640 mS. For normal servo control applications, 10 ms is suggested. ***The watchdog disable feature is for manual testing and should not be used for servo control applications.***

The analog outputs are cleared by resetting theAD5754 DAC chip. If this happens, the DAC chip must be re-initialized with the desired mode and range information for proper watchdog timeout recovery.

UPDATE RATE

The 7I65 is suitable for servo systems with analog output update rates up to approximately 60 KHz. At lower update rates (10KHz and below) all analog input channels can be read at the update rate if desired. Due to the overhead of ADC reading, maximum update rates may require that the ADC be read in an interleaved fashion, that is only one ADC channel read per update loop, for example:

OUTPUT DAC0 DATA	OUTPUT DAC1 DATA
OUTPUT DAC2 DATA	OUTPUT DAC3 DATA
OUTPUT DAC4 DATA	OUTPUT DAC5 DATA
OUTPUT DAC6 DATA	OUTPUT DAC7 DATA
OUTPUT ENABLE DATA	READ ONE ADC CHANNEL

OPERATION

BSPI INTERFACE

The 7I65 will often be used the HostMot2 FPGA configuration, and specifically HostMot2's BSPI module. The BSPI module is a FIFO buffered master SPI interface. The BSPI interface supports multiple different SPI devices on a single channel, and is a good match for the 7I65. The BSPI module uses channel descriptor registers to setup the SPI interface for each device type, and possibly for different SPI transactions to a single device. The following is a brief BSPI register description:

BSPI DATA FIFO

The SPI data FIFO is the location of a 16 deep transmit and 16 deep receive FIFO for the SPI interface. There is only one transmit and one receive FIFO per buffered SPI interfacebut the FIFO interface spans 16 doublewords of address space. This is so that when data is written to the FIFO, the address bits are written into the FIFO as well. These address bits select the channel descriptor at the SPI end of the transmit FIFO. The receive FIFO also spans the same address space but the read address within the range is dont-care.

BSPI CHANNEL DESCRIPTOR SETUP

The channel descriptor setup location is where the channel descriptors for up to 16 SPI peripherals are written. The channel descriptors are written in last to first order, in other words, to setup 9 channel descriptors, first the channel descriptor for SPI device 9 is written, then the channel descriptor for SPI device 8 is written, repeating the decending device order until the channel descriptor for SPI device 0 is written.

BSPI CHANNEL DESCRIPTOR FIELDS

Bits 0..5 = bits per SPI frame (bits = N+1) ie 0x1f = 32 bit frame

Bit 6 = CPOL = Clock polarity (FreeScale SPI spec compatible definitions)

Bit 7 = CPHA = Clock Phase

Bits 8..15 = Programmable divider, SPI bit rate is CLOCKLOW/((N+1)*2)

Bits 16..19 = Chip select bits for SPI interface

Bits 24..28 = Chip select delay = chip select valid delay before and after frame in (N+1 CLOCKLOW periods, N = 0 ..15 n>15 = 0 delay.

Bit 30 = Dont_Clear_Frame. If set, leave frame asserted at.

Bit 31 = Dont_Echo. If set, dont push SPI returned data on receive FIFO. (for output only SPI devices)

OPERATION

BSPI INTERFACE

BSPI FIFO COUNT REGISTER

The FIFO count register show the current transmit and receive FIFO data counts. If data is written to the FIFO count register, both transmit and receive FIFOs are cleared, (write data is dont-care)

Bits 0..4 = Receive FIFO data counter

Bits 8..12 = Transmit FIFO data counter

SUGGESTED BSPI CHANNEL DESCRIPTOR VALUES

The following table shows appropriate channel descriptor register values for the 7I65 when used with a FPGA card with 48 or 50 MHz ClockLow (4I68,7I43,5I22,5I23):

DEVICE	Chan descriptor	Channel descriptor function
CS0 = loopback	0x1000055F	Echo, CS0, ~ 4 MHz, CPOL, 32 bits
CS1 = AD5754	0x90010057	No echo, CS1, 24/25 MHz, CPOL, 24 bits
CS2 = AD5754	0x90020057	No echo, CS2, 24/25 MHz, CPOL, 24 bits
CS3 = AD7329	0x1003034F	Echo, CS3, ~6 MHz, CPOL, 16 bits
CS4 = CPLD	0x1004034B	Echo, CS4, ~6 MHz, CPOL, 12 bits
CS5 = Not Used	0x90050041	No echo, CS5, 24/25 MHz, 2 bits
CS6 = Not Used	0x90060041	No echo, CS5, 24/25 MHz, 2 bits
CS7 = EEPROM	0x100705C7	Echo, CS7, ~4 MHz, CPOL,CPHA, 8 bits
CS7 = EEPROM	0x900705C7	No Echo, CS7, ~4 MHz, CPOL,CPHA, 8 bits
CS7 = EEPROM	0xD00705C7	No Echo, DontClearFrame, CS7, ~4 MHz, CPOL,CPHA, 8 bits

Note that the EEPROM has multiple length SPI frames, some longer than 32 bits. Multiple descriptors for the EEPROM are used simplify the EEPROM interface. Frames longer than 32 bits are handled by using the DontClearFrame option bit in the descriptor. For example, a EEPROM byte write requires 5 bytes, a write command, a 3 byte address, and the data byte. These are sent as 5 individual bytes, the first four with using the descriptor with the DontClearFrame option bit and the last using the descriptor without the DontClearFrame, generating a 40 bit frame.

OPERATION

BSPI INTERFACE

SUGGESTED BSPI CHANNEL DESCRIPTOR VALUES

The following table shows appropriate channel descriptor register values for the 7I65 when used with a FPGA card with 33 MHz ClockLow (4I65,5I20):

DEVICE	Chan descriptor	Channel descriptor function
CS0 = loopback	0x1000035F	Echo, CS0, ~ 4 MHz, CPOL, 32 bits
CS1 = AD5754	0x90010057	No echo, CS1, ~16 MHz, CPOL, 24 bits
CS2 = AD5754	0x90020057	No echo, CS2, ~16 MHz, CPOL, 24 bits
CS3 = AD7329	0x1003024F	Echo, CS3, ~5 MHz, CPOL, 16 bits
CS4 = CPLD	0x1004024B	Echo, CS4, ~5 MHz, CPOL, 12 bits
CS5 = Not Used	0x90050041	No echo, CS5, ~16 MHz, 2 bits
CS6 = Not Used	0x90060041	No echo, CS5, ~16 MHz, 2 bits
CS7 = EEPROM	0x100703C7	Echo, CS7, ~4 MHz, CPOL,CPHA, 8 bits
CS7 = EEPROM	0x900703C7	No Echo, CS7, ~4 MHz, CPOL,CPHA, 8 bits
CS7 = EEPROM	0xD00703C7	No Echo, DontClearFrame, CS7, ~4 MHz, CPOL,CPHA, 8 bits

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	+4.75	+5.25	VDC
5V POWER CONSUMPTION	---	250	mA
(no external load)			
ANALOG OUTPUT VOLTAGE ACCURACY	—	.2	%
ANALOG OUTPUT RESOLUTION	—	16	bits
ANALOG OUTPUT LINEARITY	—	12	bits
ANALOG OUTPUT RIPPLE AND NOISE	—	1	mV P-P
(0-100 KHz bandwidth)			
MINIMUM AOUT LOAD RESISTANCE	2K	---	Ohm
(Total +- supply current must be less than 24 mA.)			
ANALOG INPUT VOLTAGE ACCURACY	—	.2	%
ANALOG INPUT RESOLUTION	—	12	bits
(ADC is 12 bits + sign, this is sometimes called a 13 bit ADC)			
ENABLE OUTPUT SWITCH VOLTAGE	-.3	+30	VDC
ENABLE OUTPUT SWITCH CURRENT	—	5	mA
(Current for .4V maximum on state voltage)			
MISC INPUT SENSE VOLTAGE	4	24	VDC

SPECIFICATIONS

	MIN	MAX	UNITS
ENCODER FREQUENCY (TTL)	DC	1	MHz
ENCODER FREQUENCY (RS-422)	DC	5-8	MHz
(quadrature encoder filter disabled)			
ENCODER FREQUENCY (RS-422)	DC	1-1.6	MHz
(quadrature encoder filter enabled)			
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND