7I48 MANUAL

Six channel analog servo amp interface

V1.6

This page intentionally almost blank

Table of Contents

GENERAL 1

DESCRIPTION 1

HARDWARE CONFIGURATION 2

DEFAULT JUMPER LOCATIONS 2
TTL/RS-422 ENCODER SELECTION 2
CABLE POWER/P1 POWER SELECTION 2

CONNECTORS 3

CONNECTOR LOCATIONS AND DEFAULT JUMPERS 3
CONTROLLER CONNECTOR 4
AUX 5V POWER 4
SERVO AMP/ENCODER CONNECTORS 5

OPERATION 8

PWM RATE 8
STEP RESPONSE 8
ENCODER INPUT CIRCUIT 8
MAXIMUM COUNT RATE 8
5V POWER 9
ENABLE INPUTS 9
ENABLE OUTPUTS 9
ANALOG OUTPUTS 9

SPECIFICATIONS 10
DRAWINGS 11

GENERAL

DESCRIPTION

The 7I48 is a 6 axis analog servo interfaces intended for operation with MESA's Anything I/O cards when used for motion control applications. The 7I48 uses encoder multiplexing to allow a single Anything-I/O connector to support a six axis interface.

The 7I48 takes up/down PWM or PDM signals from the Anything I/O card and converts them to +- 10V analog output voltages for direct connection to analog input servo amplifiers. The 7I48 models also conditions and multiplexes the encoder input signals with input buffers for TTL inputs a RS-422 receivers for differential encoder inputs.

The controller connection is a 50 pin header that matches the pinout of the Mesa anything I/O series of cards. The 7I48 uses Phoenix compatible 3.5 mm headers and is supplied with pluggable terminal blocks.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I48 card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side,

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W1	CABLE POWER SELECT	RIGHT = CABLE POWER
W13,W16,W19	CH0 TTL/RS-422 SELECT	LEFT = TTL
W4,W7,W10	CH1 TTL/RS-422 SELECT	LEFT = TTL
W12,W15,W18	CH2 TTL/RS-422 SELECT	LEFT = TTL
W3,W6,W9	CH3 TTL/RS-422 SELECT	LEFT = TTL
W11,W14,W17	CH4 TTL/RS-422 SELECT	LEFT = TTL
W2,W5,W8	CH5 TTL/RS-422 SELECT	LEFT = TTL

TTL/RS-422 ENCODER SELECTION

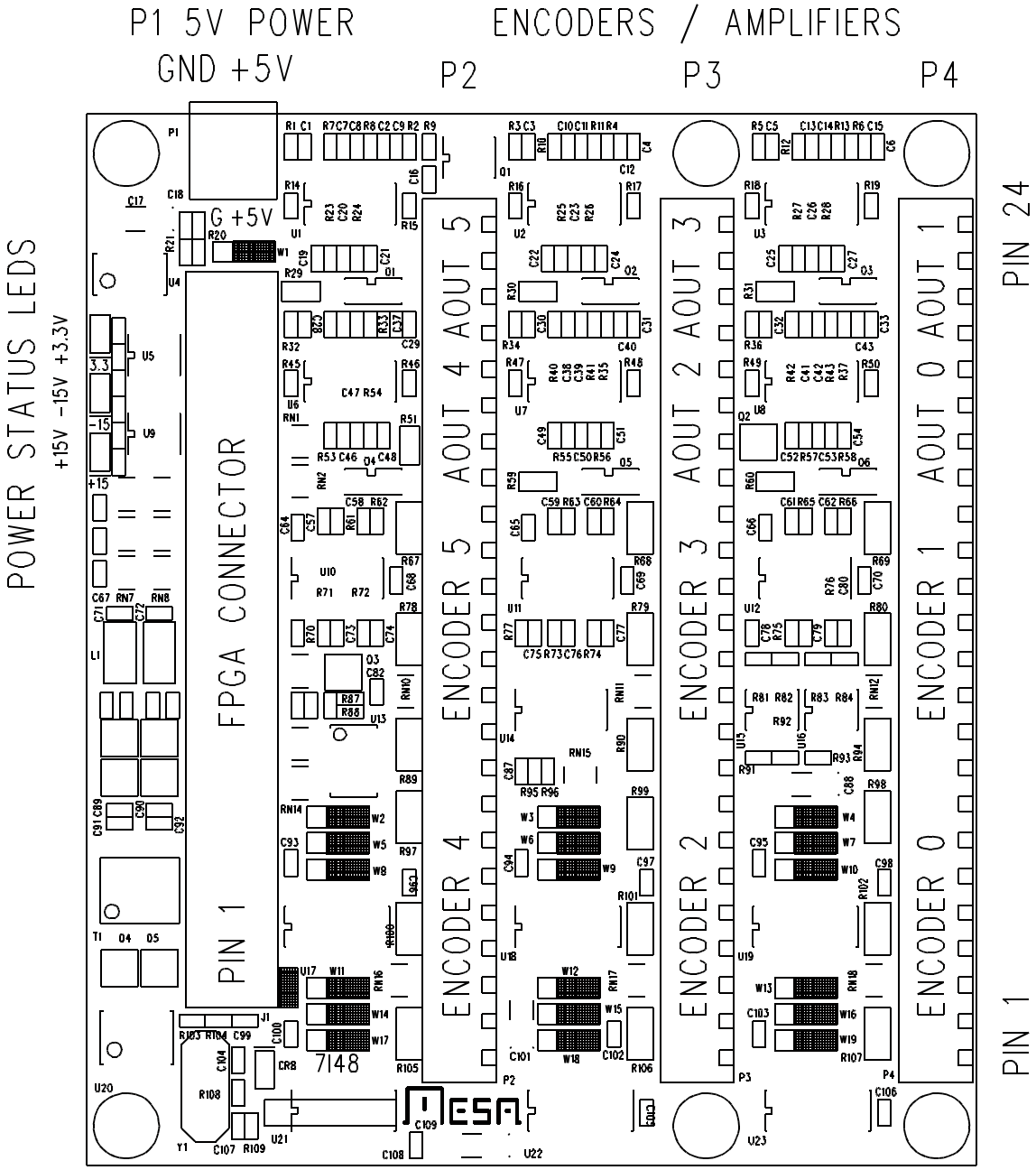
Each 7I48 channel has a selectable TTL or RS-422 (differential) encoder input conditioning. Conditioning type is determined by setting groups of 3 jumpers to the left or right position. When the jumpers are in the "LEFT" position, TTL inputs are selected, When the jumpers are in the "RIGHT" position, RS-422 inputs are selected. Note these sets of three jumpers are in physical proximity to the terminal block encoder connections.

CABLE POWER/P1 POWER SELECTION

The 7I48 can get its operating power from the flat FPGA cable or from P1. For testing and with very low power encoders, cable power can be used. W1 selects whether cable power connects to the 7I48s 5V supply. If W1 is in the "RIGHT" position, cable power is selected. If W1 is in the "LEFT" position, external 5V power must be supplied via P1.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector J1 connects to the anything I/O card/motion controller. This can be a male 50 pin header on the top of the 7I48 card or a female 50 conductor header on the bottom side of the 7I48 depending on 7I48 model. Controller connector pin-out is as follows:

PIN	FUNCTION	DIRECTION	PIN	FUNCTION	DIRECTION
1	/ENA0	TO 7I48	25	PWM-0	TO 7I48
3	MUXQA0	FROM 7I48	27	PWM+1	TO 7I48
5	MUXQB0	FROM 7I48	29	PWM-1	TO 7I48
7	MUXIDX0	FROM 7I48	31	PWM+2	TO 7I48
9	MUXQA1	FROM 7I48	33	PWM-2	TO 7I48
11	MUXQB1	FROM 7I48	35	PWM+3	TO 7I48
13	MUXIDX1	FROM 7I48	37	PWM-3	TO 7I48
15	MUXQA2	FROM 7I48	39	PWM+4	TO 7I48
17	MUXQB2	FROM 7I48	41	PWM-4	TO 7I48
19	MUXIDX2	FROM 7I48	43	PWM+5	TO 7I48
21	MUXSEL0	TO 7I48	45	PWM-5	TO 7I48
23	PWM+0	TO 7I48	47	/ENA1	TO 7I48
			49	+5V PWR	TO 7I48

Note: all even pins are grounded.

AUX 5V POWER

The 7I48 can get its 5V power from the FPGA cable or connector P1. Normally P1 should be used for power as the 5V current draw from 6 encoders will exceed what the FPGA flat cable can deliver. Note that the 7I48 will only connect to P1 power if the cable 5V is present.

PIN	FUNCTION
1	5V
2	GND

CONNECTORS

SERVO AMP/ENCODER CONNECTORS

The 7I48's servo amplifier / encoder connectors (P2,P3, and P4) are 3.5MM 24 pin headers compatible with Phoenix style screw terminal blocks (supplied). Connector P4 has the I/O signals for channels 0 and 1:

P4 PIN	FUNCTION	DIR
1	ENCA0	TO 7I48
2	/ENCA0	TO 7I48
3	GND	FROM 7I48
4	ENCB0	TO 7I48
5	/ENCB0	TO 7I48
6	+5V	FROM 7I48
7	IDX0	TO 7I48
8	/IDX0	TO 7I48
9	ENCA1	TO 7I48
10	/ENCA1	TO 7I48
11	GND	FROM 7I48
12	ENCB1	TO 7I48
13	/ENCB1	TO 7I48
14	+5V	FROM 7I48
15	IDX1	TO 7I48
16	/IDX1	TO 7I48
17	ENA0-	FROM 7I48
18	ENA0+	FROM 7I48
19	GND0	FROM 7I48
20	AOUT0	FROM 7I48
21	ENA1-	FROM 7I48
22	ENA1+	FROM 7I48
23	GND1	FROM 7I48
24	AOUT1	FROM 7I48

CONNECTORS

SERVO AMP/ENCODER CONNECTORS

Connector P3 has the I/O signals for channels 2 and 3:

P3 PIN	FUNCTION	DIR
1	ENCA2	TO 7I48
2	/ENCA2	TO 7I48
3	GND	FROM 7I48
4	ENCB2	TO 7I48
5	/ENCB2	TO 7I48
6	+5V	FROM 7I48
7	IDX2	TO 7I48
8	/IDX2	TO 7I48
9	ENCA3	TO 7I48
10	/ENCA3	TO 7I48
11	GND	FROM 7I48
12	ENCB3	TO 7I48
13	/ENCB3	TO 7I48
14	+5V	FROM 7I48
15	IDX3	TO 7I48
16	/IDX3	TO 7I48
17	ENA2-	FROM 7I48
18	ENA2+	FROM 7I48
19	GND2	FROM 7I48
20	AOUT2	FROM 7I48
21	ENA3-	FROM 7I48
22	ENA3+	FROM 7I48
23	GND3	FROM 7I48
24	AOUT3	FROM 7I48

CONNECTORS

SERVO AMP/ENCODER CONNECTORS

Connector P2 has the I/O signals for channels 4 and 5:

P2 PIN	FUNCTION	DIR
1	ENCA4	TO 7I48
2	/ENCA4	TO 7I48
3	GND	FROM 7I48
4	ENCB4	TO 7I48
5	/ENCB4	TO 7I48
6	+5V	FROM 7I48
7	IDX4	TO 7I48
8	/IDX4	TO 7I48
9	ENCA5	TO 7I48
10	/ENCA5	TO 7I48
11	GND	FROM 7I48
12	ENCB5	TO 7I48
13	/ENCB5	TO 7I48
14	+5V	FROM 7I48
15	IDX5	TO 7I48
16	/IDX5	TO 7I48
17	ENA4-	FROM 7I48
18	ENA4+	FROM 7I48
19	GND4	FROM 7I48
20	AOUT4	FROM 7I48
21	ENA5-	FROM 7I48
22	ENA5+	FROM 7I48
23	GND5	FROM 7I48
24	AOUT5	FROM 7I48

OPERATION

PWM RATE

The 7I48 is meant to operate with PWM rates from 24 KHz to 500 KHz. Operation at lower PWM rates will result in excessive output ripple, operation at higher PWM rates or with PDM with higher than 10 MHz base frequency will result in poor linearity. When used with HostMot2 firmware, the PWM generators should be set for UP/DOWN mode (mode 2) and the PWM frequency set for 24 KHz.

STEP RESPONSE

The 7I48 has a 5 pole PWM filter with an approximate 150 uSec time constant. This value is selected as a compromise between output ripple and settling time. This is much faster than most controlled devices and will not normally have any effect on loop stability or performance. The 7I48 can be assembled with different components if necessary to change this time constant.

ENCODER INPUT CIRCUIT

The 7I48 input circuit is different depending on whether TTL or RS-422 encoder types have been selected. In TTL mode the input circuit on the encoder A,B, and index inputs drive one input of the RS-422 differential receiver, and the other receiver input is terminated to a 1.6V (TTL threshold) reference voltage. In RS-422 mode, the input consists of a 132 Ohm termination resistor and a 26LS32 RS-422 differential receiver.

When TTL encoders are used, they connect to the 'True' input of the differential pair, for example a TTL encoder for channel 2 would connect to ENCA2, ENCB2 and IDX2, while the /ENCA2,/ENCB2, and /IDX2 terminals would be left open.

Fine print: normally the input mode jumpers would always be moved as a sets of three to select TTL or RS-422 mode for individual encoders, however it is possible to select TTL or RS-422 mode for each encoder signal, for example if a encoder had a differential A,B but TTL index, the input circuit can accommodate this. The three input mode select jumpers are in bottom to top order: A,B,INDEX.

MAXIMUM COUNT RATE

The 7I48 uses multiplexed encoder signals to save interface pins. The multiplexing rate will determine the maximum encoder count rate. Default multiplexing rate with HostMot2 firmware is ClockLow / 8, or approximately 4 or 6 MHz, giving a resolvable count rate of 2 to 3 MHz. Multiplexing rate can be increased if desired but high multiplex rates will require short cables between the FPGA controller card and the 7I48 due to signal integrity and time-of-flight considerations. Maximum practical multiplex rate is approximately 12 MHz (and 6 MHz count rates). Encoder count rate is further limited by HostMot2s input filtering to ~5 to ~8 million counts per second (encoder filtering off) and ~1 to ~1.6 million counts per second (encoder filtering on).

OPERATION

5V POWER

The 7I48 requires ~400 mA of 5V power for operation. Encoder power can also be supplied from the 7I48's 5V source. Power for the 7I48 is normally supplied from P1 but can also be supplied via pin 49 of the 50 conductor controller cable when testing or when low power encoders are used.

ENABLE INPUTS

There are two active low enable inputs on the 7I48 from the FPGA card. When either of these enable inputs is high, all AOUTs are forced to 0V, and all enable outputs are turned off. Pullup resistors keep the enable inputs high if the controller connection is lost.

ENABLE OUTPUTS

Each 7I48 channel has a OPTO-isolated transistor output that can be used to enable external amplifiers. All six outputs are on when both input enable signals are low, that is all enable outputs are switched at once. Maximum switched voltage is 36VDC. Maximum output current is 10 mA. Even though all outputs are switched in common, they are all isolated to allow different enable connections on a per amplifier basis.

Example connections:

1. Active high 12V amplifier enable on ch 0:

    Connect ENA0+ to +12V source

    Connect ENA0- to amplifier enable input

2. Active low TTL input

    Connect ENA2- to ground

    Connect ENA2+ to amplifier enable input

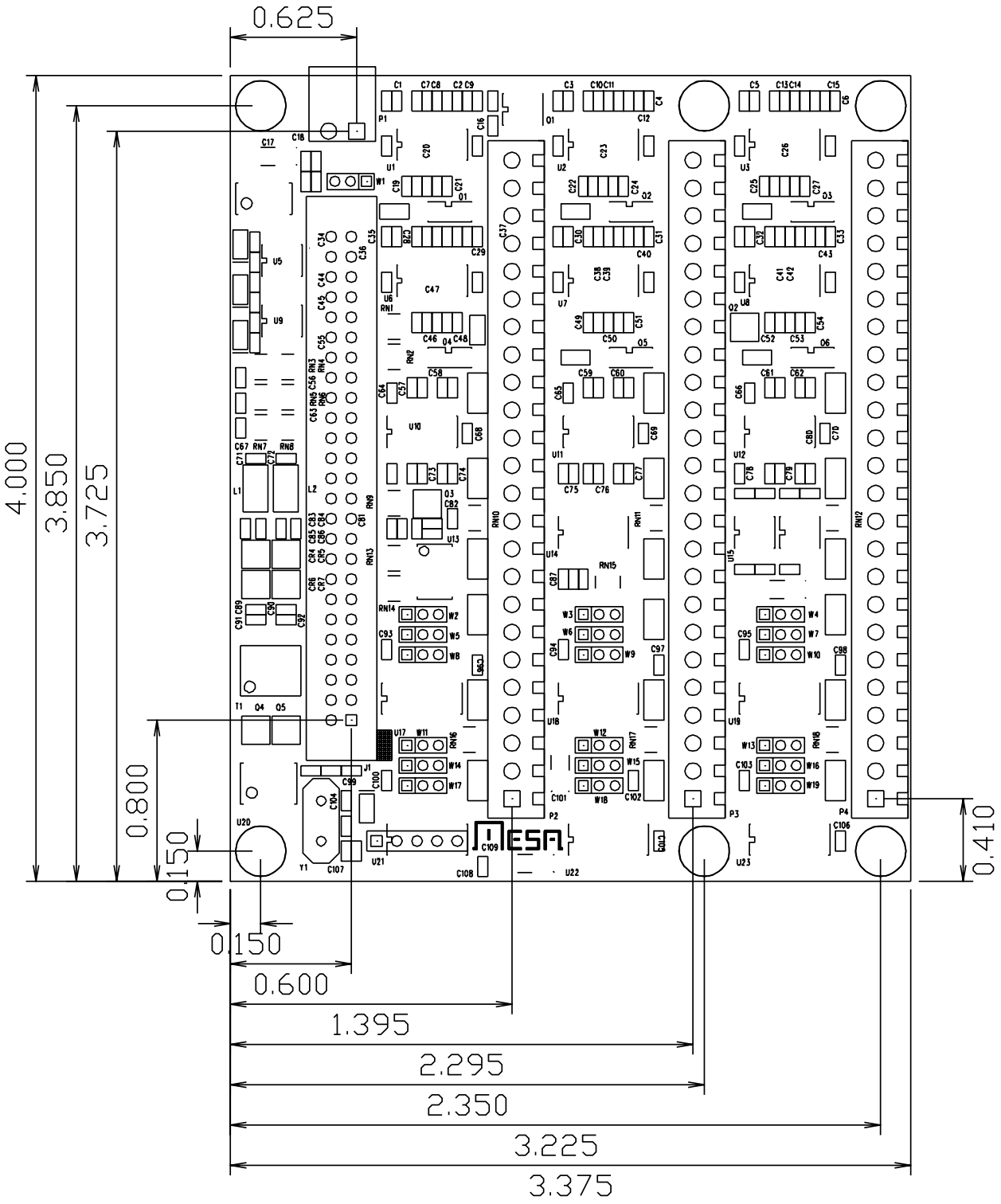
ANALOG OUTPUTS

The analog output of the 7I48 swings from -10 v to +10V. Positive outputs are generated when PWM+ is input is driven, and negative outputs when PWM- is driven. A 50 % duty cycle PWM signal will generate a 5V output. This mode of operation require the PWM generator be set for "up/down" mode. *Due to power supply limitations, The 7I48 has limited DC output drive capability and should not have loads of less than 3K Ohms on its analog outputs. (~24 mA maximum total +-10v current). To avoid power supply damage, do no short more than one analog output at once*.

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.75	5.25	VDC
5V POWER CONSUMPTION	---	500	mA
(no external load)			
ANALOG OUTPUT VOLTAGE	+-9.8	+-10.2	V
ANALOG OUTPUT STEP RESPONSE	120	160	uSec
MINIMUM AOUT LOAD RESISTANCE	3K	---	Ohm
OUTPUT RIPPLE @ 24 KHZ PWM	---	.1%	% FS
LINEARITY	---	.1%	% FS
(no missing codes, 13 bit resolution with 24 KHz PWM)			
ZERO OFFSET ERROR	-10	+10	mV
ENCODER FREQUENCY	DC	4	MHz
(8 MHz multiplex frequency selected)			
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND

DRAWINGS


0.625
4.000
3.850
3.725
0.800
0.150
0.150
0.600
1.395
2.295
2.350
3.225
3.375
0.410