

7147S MANUAL

8/12 channel motion oriented differential interface with analog out

V1.0

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GENERAL

DESCRIPTION

The 7I47S is a 12 input, 8 output RS-422 interface for Mesa's Anything I/O series of FPGA interface cards. The 7I47 has 12 receive and 8 transmit channels plus a analog output intended for spindle speed control. The 7I47S is mainly intended for motion oriented applications, for example as an output buffer and line receiver for connecting step and direction drives and encoders to Anything I/O FPGA cards.

The controller connection is a 50 pin header that matches the pinout of Mesa's Anything I/O cards. All RS-422 interface connections use pluggable Phoenix compatible 3.5 mm screw terminals.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I47S card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side.

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W1	CABLE/AUX 5V POWER	LEFT = CABLE POWER
W4	RX11	LEFT = TERM
W5	RX5	LEFT = TERM
W6	RX10	LEFT = TERM
W7	RX4	LEFT = TERM
W8	RX9	LEFT = TERM
W9	RX3	LEFT = TERM
W10	RX8	LEFT = TERM
W11	RX2	LEFT = TERM
W12	RX7	LEFT = TERM
W13	RX1	LEFT = TERM
W14	RX6	LEFT = TERM
W15	RX0	LEFT = TERM

TERMINATION ENABLE

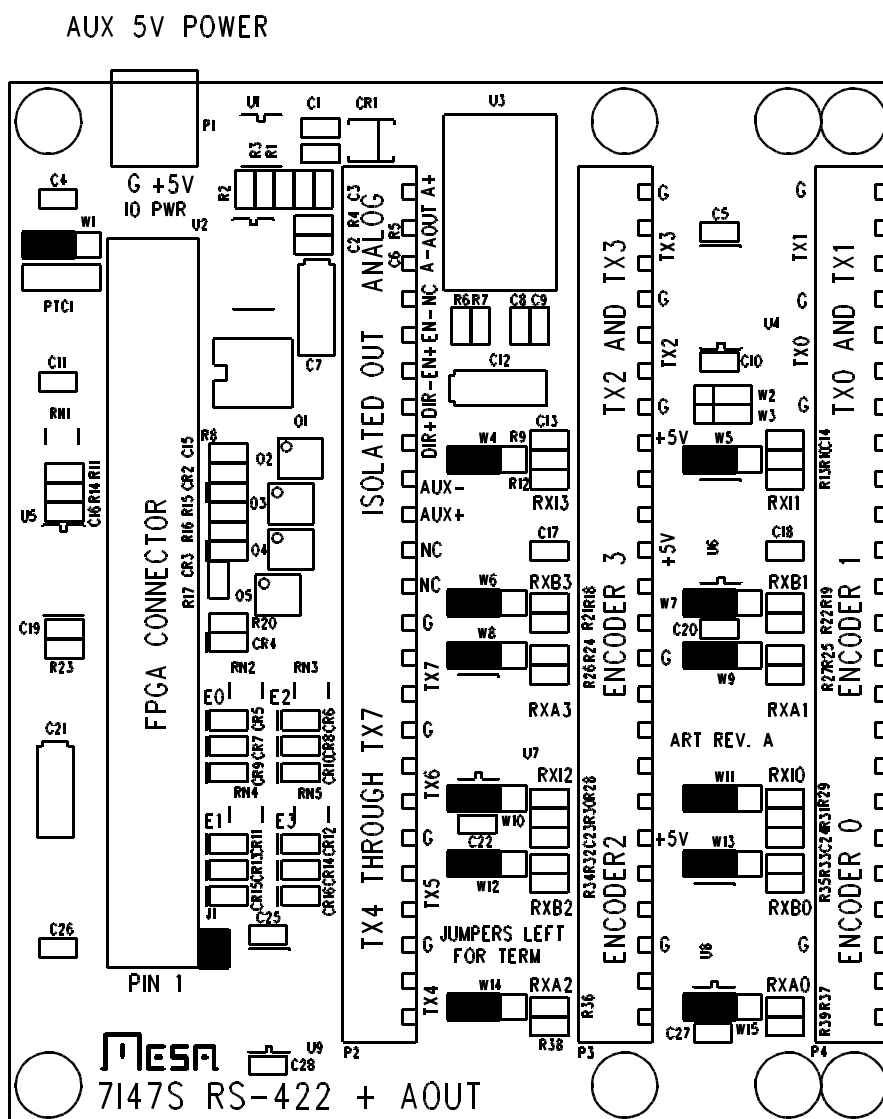
The 7I47S can terminate its RS-422 inputs if desired. Termination is enabled by setting the appropriate jumper to the left hand position. If termination is not desired, the jumper should be moved to the right hand position.

CABLE POWER ENABLE

The 7I47S can supply I/O power to P3 and P4 via P1 or via the 50 conductor flat cable. If W1 is in the left hand position, flat cable power is used. If W1 is on the right hand position, P1 power is used.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector J1 connects to the anything I/O card/motion controller. This can be a male 50 pin header on the top of the 7I47S card or a female 50 conductor header on the bottom side of the 7I47S depending on 7I47S model.

PIN	FUNCTION	DIRECTION	PIN	FUNCTION	DIRECTION
1	TX4	TO 7I47S	25	RX4	FROM 7I47S
3	TX5	TO 7I47S	27	RX10	FROM 7I47S
5	TX6	TO 7I47S	29	RX5	FROM 7I47S
7	TX7	TO 7I47S	31	RX11	FROM 7I47S
9	RX0	FROM 7I47S	33	AUX	TO 7I47S
11	RX6	FROM 7I47S	35	DIR	TO 7I47S
13	RX1	FROM 7I47S	37	/ENA	TO 7I47S
15	RX7	FROM 7I47S	39	PWM	TO 7I47S
17	RX2	FROM 7I47S	41	TX0	TO 7I47S
19	RX8	FROM 7I47S	43	TX1	TO 7I47S
21	RX3	FROM 7I47S	45	TX2	TO 7I47S
23	RX9	FROM 7I47S	47	TX3	TO 7I47S
			49	+5V PWR	TO 7I47S

Note: all even pins are grounded. Alternate encoder names omitted for space

AUX 5V POWER

2 pin pluggable terminal P1 can be used to supply 5V power to the I/O terminals on the 7I47S. This is suggested for most applications as the encoders typically will draw more current than can be supplied via the FPGA flat cable. P1 has the following pinout:

PIN	FUNCTION
1	5V
2	GND

CONNECTORS

RS-422 CONNECTOR P4

Connector P4 is a 3.5MM pluggable screw terminal block with the following pinout:

P4 PIN	FUNCTION	DIR
1	RX0	TO 7I47S
2	/RX0	TO 7I47S
3	GND	FROM 7I47S
4	RX1	TO 7I47S
5	/RX1	TO 7I47S
6	+5V	FROM 7I47S
7	RX2	TO 7I47S
8	/RX2	TO 7I47S
9	RX3	TO 7I47S
10	/RX3	TO 7I47S
11	GND	FROM 7I47S
12	RX4	TO 7I47S
13	/RX4	TO 7I47S
14	+5V	FROM 7I47S
15	RX5	TO 7I47S
16	/RX5	TO 7I47S
17	+5V	FROM 7I47S
18	GND	FROM 7I47S
19	TX0	FROM 7I47S
20	/TX0	FROM 7I47S
21	GND	FROM 7I47S
22	TX1	FROM 7I47S
23	/TX1	FROM 7I47S
24	GND	FROM 7I47S

Note that actual signal functions depend on FPGA configuration.

CONNECTORS

RS-422 CONNECTOR P3

Connector P4 is a 3.5MM pluggable screw terminal block with the following pinout:

P3 PIN	FUNCTION	DIR
1	RX6	TO 7I47S
2	/RX6	TO 7I47S
3	GND	FROM 7I47S
4	RX7	TO 7I47S
5	/RX7	TO 7I47S
6	+5V	FROM 7I47S
7	RX8	TO 7I47S
8	/RX8	TO 7I47S
9	RX9	TO 7I47S
10	/RX9	TO 7I47S
11	GND	FROM 7I47S
12	RX10	TO 7I47S
13	/RX10	TO 7I47S
14	+5V	FROM 7I47S
15	RX11	TO 7I47S
16	/RX11	TO 7I47S
17	+5V	FROM 7I47S
18	GND	FROM 7I47S
19	TX2	FROM 7I47S
20	/TX2	FROM 7I47S
21	GND	FROM 7I47S
22	TX3	FROM 7I47S
23	/TX3	FROM 7I47S
24	GND	FROM 7I47S

Note that actual signal functions depend on FPGA configuration.

CONNECTORS

RS-422/ANALOG CONNECTOR P2

Connector P2 is a 3.5MM pluggable screw terminal block with the following pinout:

P2 PIN	FUNCTION	DIR	TYPE
1	TX4	FROM 7I47S	RS-422
2	/TX4	FROM 7I47S	RS-422
3	GND	FROM 7I47S	RS-422
4	TX5	FROM 7I47S	RS-422
5	/TX5	FROM 7I47S	RS-422
6	GND	FROM 7I47S	RS-422
7	TX6	FROM 7I47S	RS-422
8	/TX6	FROM 7I47S	RS-422
9	GND	FROM 7I47S	RS-422
10	TX7	FROM 7I47S	RS-422
11	/TX7	FROM 7I47S	RS-422
12	GND	FROM 7I47S	RS-422
13	NC	FROM 7I47S	
14	NC	FROM 7I47S	
15	AUX-	FROM 7I47S	OPTO OUTPUT-
16	AUX+	FROM 7I47S	OPTO OUTPUT+
17	DIR-	FROM 7I47S	OPTO OUTPUT-
18	DIR+	FROM 7I47S	OPTO OUTPUT+
19	ENA-	FROM 7I47S	OPTO OUTPUT-
20	ENA+	FROM 7I47S	OPTO OUTPUT+
21	NC	FROM 7I47S	
22	ANALOG -	TO 7I47S	ANALOG REFERENCE -
23	ANALOG OUT	FROM 7I47S	ANALOG OUT (WIPER)
24	ANALOG+	TO 7I47S	ANALOG REFERENCE +

Note that actual signal functions depend on FPGA configuration.

OPERATION

5V POWER

The 7I47S requires ~100 mA of 5V power for operation. This power will increase based on the number of terminated TX outputs used, up to a maximum of ~400 mA.

Power for the 7I47S logic is normally supplied from pin 49 of the 50 conductor controller cable. P1 supplies power only to the 5V I/O terminals on P3 and P4 (chiefly for encoder power).

If W1 is on the left hand position, the controller cable will supply both the logic and I/O power and P1 can remain unconnected. This mode can be used for testing but it is suggested that W1 be placed in the right hand position and I/O power be supplied via P1 for most applications.

The power from connector P1 Passes through a 1.3A PTC device before being routed to the I/O terminals. This limits the total I/O power supplied by the 7I47S to ~800 mA in 0 to 70C ambients.

OUTPUT DRIVE

The 7I47Ss outputs are designed to drive singly terminated RS-422 lines or remote opto-isolator diodes. Maximum output drive is 35 mA. The 7I47S outputs can be used individually for interfacing single ended loads. Unloaded outputs swing to 5V (Full 5V CMOS outputs)

INPUT/OUTPUT POLARITY

The RS-422 differential I/O signals consists of a inverted and non-inverted signal pair for each unbalanced signal on the Anything I/O side of the interface. The TX(N) and RX(N) signals are the inverted signals. The /TX(N) and /RX(N) signals are the non-inverted RS-422 signals. This seemingly inverted convention is used to maintain compatibility with encoder inputs on other Mesa products and RS-422 serial usage. For driving single ended loads, either the inverting or non-inverting output may be chosen.

MONITOR / ENCODER LEADS

Monitor LEDs are provided on the RX(N) lines, especially for use with encoder inputs. These LEDs are arranged in 4 groups of 3 to monitor the A/B/INDEX lines of 4 encoders.

OPERATION

ANALOG OUT

The 7I47S provides one analog output for spindle control. The analog output is a isolated potentiometer replacement type device. It functions like a potentiometer with ANALOG + being one end of the potentiometer, ANALOG OUT being the wiper and ANALOG- being the other end. The voltage on ANALOG out can be set to any voltage between ANALOG- and ANALOG+. Polarity and voltage range must always be observed for proper operation. The voltage supplied between ANALOG+ and ANALOG- must be between 5VDC and 15VDC with ANALOG + always being more positive than ANALOG-. The analog output voltage is set by PWM from the controller. The optimum PWM frequency is approximately 5KHz, Higher frequencies will have lower ripple but more non-linearity, lower frequencies will have better linearity but more ripple.

A 50% duty cycle PWM signal will result in a 50 % voltage output. The voltage output is gated by the ENABLE interface signal, and forced to = ANALOG- when enable is not asserted (enable is active low at the FPGA interface level).

Because the analog output is isolated, bipolar output is possible, for example with ANALOG+ connected to 5V and ANALOG- connected to -5V, a $\pm 5V$ analog output range is created. In this case the PWM output must be offset so that 50% PWM is generated when a 0V output is required. Note that if bipolar output is used, the output will be forced to ANALOG- at startup or when ENABLE is false.

ISOLATED OUTPUTS

The 7I47S provides 3 isolated outputs for use for spindle direction control, spindle enable or other applications. These outputs are OPTOCoupler transistors. They are all isolated from one another so can be used for pull up or pull-down individually. They will switch a maximum of 5 mA at 0 to 40VDC. The ENABLE output is special as it uses the same signal that enables the analog out. When analog output is enabled, the ENABLE OPTO output is on. The DIR and AUX outputs have no special functions so may be used for any purpose.

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.75	5.25	VDC
5V POWER CONSUMPTION	---	400	mA
(all outputs loaded with 130 ohm terminations)			
MAXIMUM POWER TO I/O CONNECTORS	---	800	mA
MAXIMUM DATA RATE	—	10	MBIT/S
RS-422 INPUT COMMON MODE RANGE	-7	+12	Volts
RS-422 INPUT TERMINATION RESISTOR	131	135	Ohm
RS-422 OUTPUT LOW (24 mA sink)	—	.8	Volts
RS-422 OUTPUT HIGH (24 mA source)	VCC-.8	—	Volts
ANALOG REFERENCE VOLTAGE	5	15	Volts
(ANALOG+ - ANALOG-)			
ANALOG SUPPLY CURRENT	—	20 mA	
ANALOG ISOLATION VOLTAGE	—	500	Volts DC
ISOLATED OUTPUT CURRENT	—	5	mA
ISOLATED OUTPUT SWITCH VOLTAGE	—	40	Volts DC
ISOLATION VOLTAGE	—	500	Volts DC
OPERATING TEMP.	0	+70	°C
OPERATING TEMP. (-I version)	-40	+85	°C
OPERATION HUMIDITY	0	95%	NON-COND