MESA

7I47 MANUAL

12 channel motion oriented differential interface

V1.5

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GENERAL

DESCRIPTION

The 7I47 is a 12 channel RS-422 interface for Mesa's Anything I/O series of FPGA interface cards. The 7I47 has 12 independent receive and transmit channels. The 7I47 is mainly intended for motion oriented applications, for example as an output buffer and line receiver for connecting step and direction drives and encoders to Anything I/O FPGA cards.

The controller connection is a 50 pin header that matches the pinout of Mesa's Anything I/O cards. All RS-422 interface connections use pluggable Phoenix compatible 3.5 mm screw terminals.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I47 card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side.

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W1	CABLE/AUX 5V POWER	LEFT = CABLE POWER
W4	RX11	LEFT = TERM
W5	RX5	LEFT = TERM
W6	RX10	LEFT = TERM
W7	RX4	LEFT = TERM
W8	RX9	LEFT = TERM
W9	RX3	LEFT = TERM
W10	RX8	LEFT = TERM
W11	RX2	LEFT = TERM
W12	RX7	LEFT = TERM
W13	RX1	LEFT = TERM
W14	RX6	LEFT = TERM
W15	RX0	LEFT = TERM

TERMINATION ENABLE

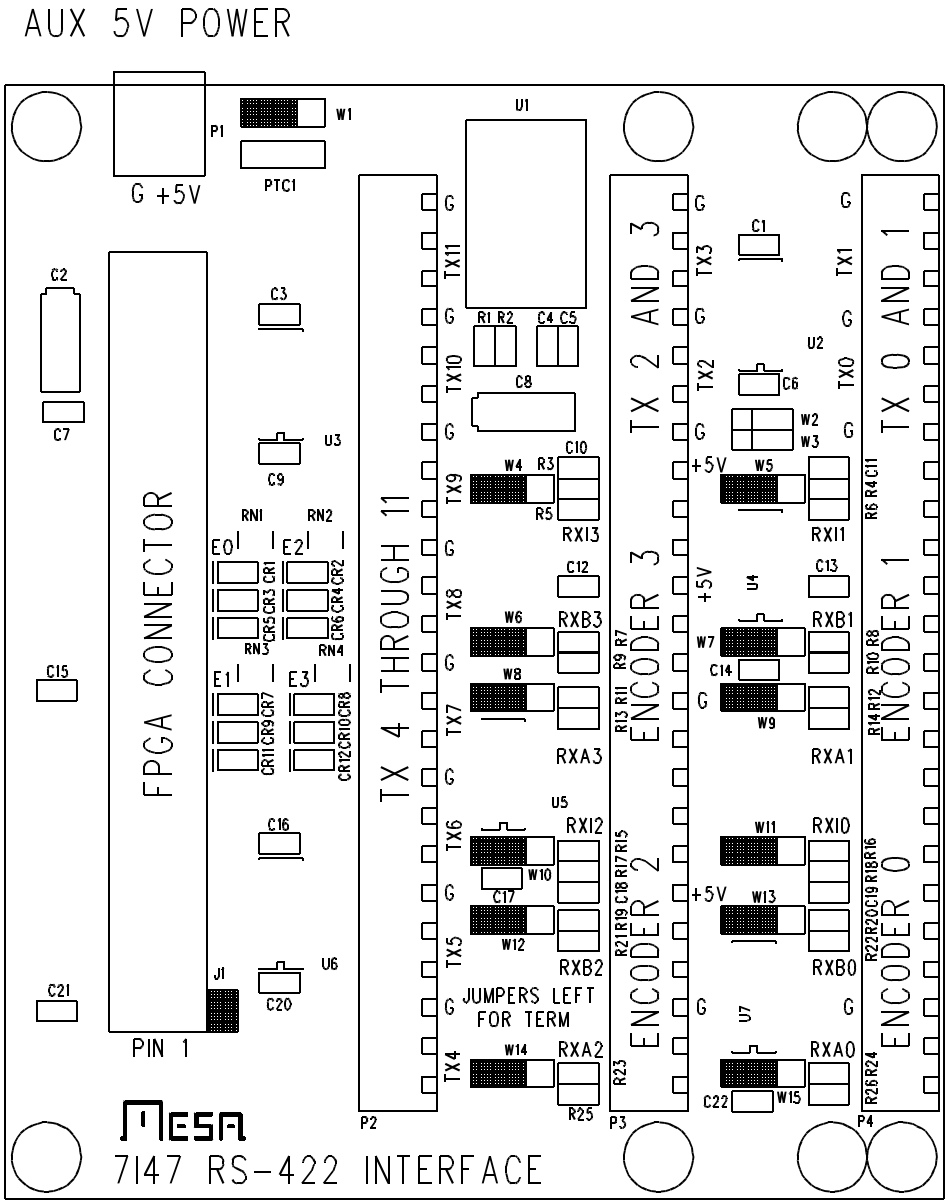
The 7I47 can terminate its RS-422 inputs if desired. Termination is enabled by setting the appropriate jumper to the left hand position. If termination is not desired, the jumper should b moved to the right hand position.

CABLE POWER ENABLE

The 7I47 can supply I/O power to P3 and P4 via P1 or via the 50 conductor flat cable. If W1 is in the left hand position, flat cable power is used. If W1 is on the right hand position, P1 power is used.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector J1 connects to the anything I/O card/motion controller. This can be a male 50 pin header on the top of the 7I47 card or a female 50 conductor header on the bottom side of the 7I47 depending on 7I47 model.

PIN	FUNCTION	DIRECTION	PIN	FUNCTION	DIRECTION
1	TX4	TO 7I47	25	RX4	FROM 7I47
3	TX5	TO 7I47	27	RX10	FROM 7I47
5	TX6	TO 7I47	29	RX5	FROM 7I47
7	TX7	TO 7I47	31	RX11	FROM 7I47
9	RX0	FROM 7I47	33	TX8	TO 7I47
11	RX6	FROM 7I47	35	TX9	TO 7I47
13	RX1	FROM 7I47	37	TX10	TO 7I47
15	RX7	FROM 7I47	39	TX11	TO 7I47
17	RX2	FROM 7I47	41	TX0	TO 7I47
19	RX8	FROM 7I47	43	TX1	TO 7I47
21	RX3	FROM 7I47	45	TX2	TO 7I47
23	RX9	FROM 7I47	47	TX3	TO 7I47
			49	+5V PWR	TO 7I47

Note: all even pins are grounded. Alternate encoder names omitted for space

AUX 5V POWER

2 pin pluggable terminal P1 can be used to supply 5V power to the I/O terminals on the7I47. This is suggested for most applications as the encoders typically will draw more current than can be supplied via the FPGA flat cable. P1 has the following pinout:

PIN	FUNCTION
1	5V
2	GND

CONNECTORS

RS-422 CONNECTOR P4

Connector P4 is a 3.5MM pluggable screw terminal block with the following pinout:

P4 PIN	FUNCTION	DIR
1	RX0	TO 7I47
2	/RX0	TO 7I47
3	GND	FROM 7I47
4	RX1	TO 7I47
5	/RX1	TO 7I47
6	+5V	FROM 7I47
7	RX2	TO 7I47
8	/RX2	TO 7I47
9	RX3	TO 7I47
10	/RX3	TO 7I47
11	GND	FROM 7I47
12	RX4	TO 7I47
13	/RX4	TO 7I47
14	+5V	FROM 7I47
15	RX5	TO 7I47
16	/RX5	TO 7I47
17	+5V	FROM 7I47
18	GND	FROM 7I47
19	TX0	FROM 7I47
20	/TX0	FROM 7I47
21	GND	FROM 7I47
22	TX1	FROM 7I47
23	/TX1	FROM 7I47
24	GND	FROM 7I47

Note that actual signal functions depend on FPGA configuration.

CONNECTORS

RS-422 CONNECTOR P3

Connector P3 is a 3.5MM pluggable screw terminal block with the following pinout:

P3 PIN	FUNCTION	DIR
1	RX6	TO 7I47
2	/RX6	TO 7I47
3	GND	FROM 7I47
4	RX7	TO 7I47
5	/RX7	TO 7I47
6	+5V	FROM 7I47
7	RX8	TO 7I47
8	/RX8	TO 7I47
9	RX9	TO 7I47
10	/RX9	TO 7I47
11	GND	FROM 7I47
12	RX10	TO 7I47
13	/RX10	TO 7I47
14	+5V	FROM 7I47
15	RX11	TO 7I47
16	/RX11	TO 7I47
17	+5V	FROM 7I47
18	GND	FROM 7I47
19	TX2	FROM 7I47
20	/TX2	FROM 7I47
21	GND	FROM 7I47
22	TX3	FROM 7I47
23	/TX3	FROM 7I47
24	GND	FROM 7I47

Note that actual signal functions depend on FPGA configuration.

CONNECTORS

RS-422 CONNECTOR P2

Connector P2 is a 3.5MM pluggable screw terminal block with the following pinout:

P2 PIN	FUNCTION	DIR
1	TX4	FROM 7I47
2	/TX4	FROM 7I47
3	GND	FROM 7I47
4	TX5	FROM 7I47
5	/TX5	FROM 7I47
6	GND	FROM 7I47
7	TX6	FROM 7I47
8	/TX6	FROM 7I47
9	GND	FROM 7I47
10	TX7	FROM 7I47
11	/TX7	FROM 7I47
12	GND	FROM 7I47
13	TX8	FROM 7I47
14	/TX8	FROM 7I47
15	GND	FROM 7I47
16	TX9	FROM 7I47
17	/TX9	FROM 7I47
18	GND	FROM 7I47
19	TX10	FROM 7I47
20	/TX10	FROM 7I47
21	GND	FROM 7I47
22	TX11	FROM 7I47
23	/TX11	FROM 7I47
24	GND	FROM 7I47

Note that actual signal functions depend on FPGA configuration.

OPERATION

5V POWER

The 7I47 requires ~100 mA of 5V power for operation. This power will increase based on the number of terminated TX outputs used, up to a maximum of ~400 mA.

Power for the 7I47 logic is normally supplied from pin 49 of the 50 conductor controller cable. P1 supplies power only to the 5V I/O terminals on P3 and P4 (chiefly for encoder power).

If W1 is on the left hand position, the controller cable will supply both the logic and I/O power and P1 can remain unconnected. This mode can be used for testing but it is suggested that W1 be placed in the right hand position and I/O power be supplied via P1 for most applications.

The power from connector P1 Passes through a 1.3A PTC device before being routed to the I/O terminals. This limits the total I/O power supplied by the 7I47 to ~800 mA in 0 to 70C ambients.

OUTPUT DRIVE

The 7I47s outputs are designed to drive singly terminated RS-422 lines or remote opto-isolator diodes. Maximum output drive is 35 mA. The 7I47 outputs can be used individually for interfacing single ended loads. Unloaded outputs swing to 5V (Full 5V CMOS outputs)

INPUT/OUTPUT POLARITY

The RS-422 differential I/O signals consists of a inverted and non-inverted signal pair for each unbalanced signal on the Anything I/O side of the interface. The TX(N) and RX(N) signals are the inverted signals. The /TX(N) and /RX(N) signals are the non-inverted RS-422 signals. This seemingly inverted convention is used to maintain compatibility with encoder inputs on other Mesa products and RS-422 serial usage. For driving single ended loads, either the inverting or non-inverting output may be chosen.

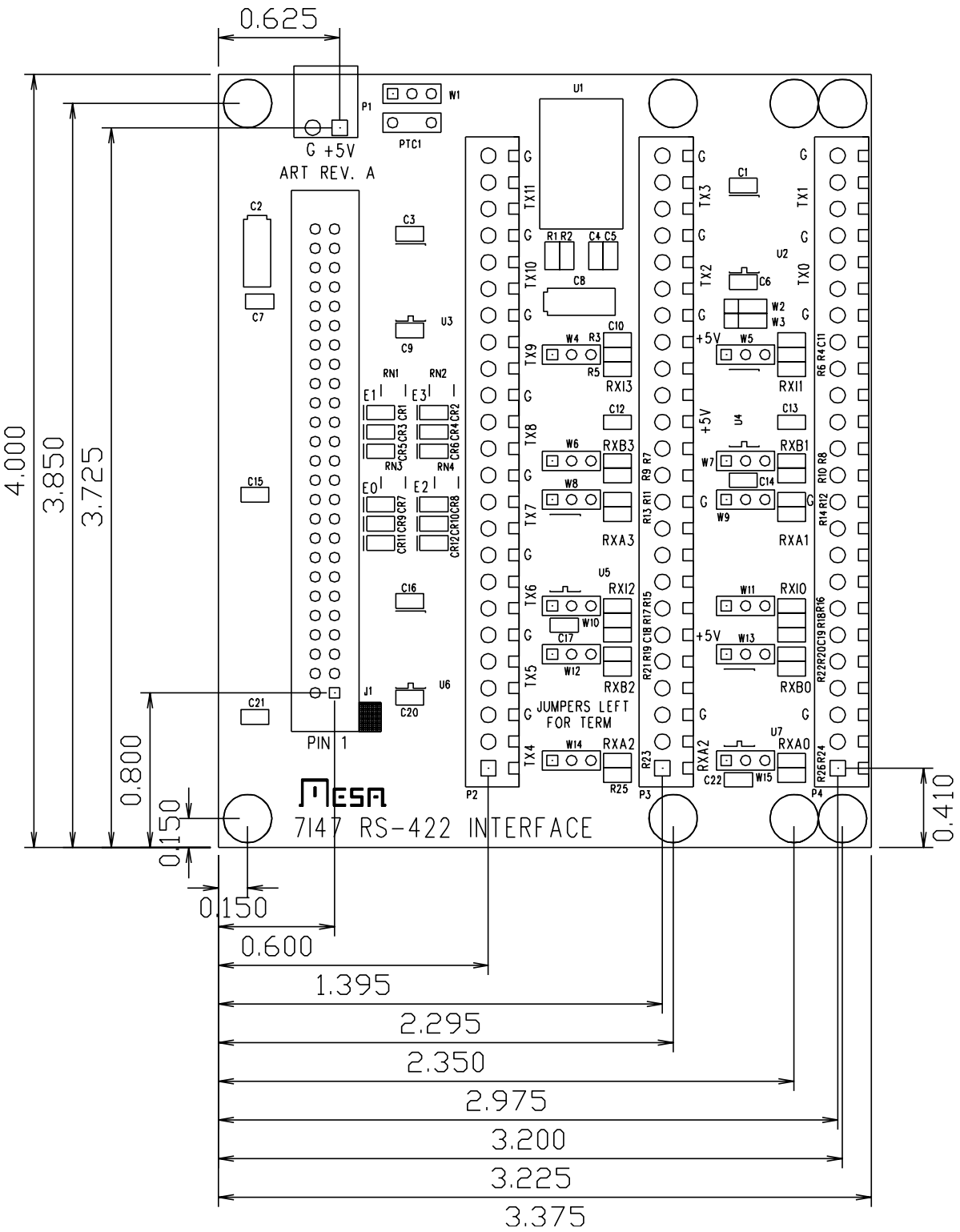
MONITOR / ENCODER LEDS

Monitor LEDs are provided on the RX(N) lines, especially for use with encoder inputs. These LEDs are arranged in 4 groups of 3 to monitor the A/B/INDEX lines of 4 encoders.

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.75	5.25	VDC
5V POWER CONSUMPTION	---	400	mA
(all outputs loaded with 130 ohm terminations)			
MAXIMUM POWER TO I/O CONNECTORS	---	800	mA
MAXIMUM DATA RATE	—	10	MBIT/S
RS-422 INPUT COMMON MODE RANGE	-7	+12	Volts
RS-422 INPUT TERMINATION RESISTOR	131	135	Ohm
RS-422 OUTPUT LOW	—	.8	Volts
(24 mA sink current)			
RS-422 OUTPUT HIGH	VCC-.8	—	Volts
(24 mA source current)			
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND

DRAWINGS


0.625
4.000
3.850
3.725
0.800
0.150
0.150
0.600
1.395
2.295
2.350
2.975
3.200
3.225
3.375
0.410
G +5V
ART REV. A
PIN 1
JUMPERS LEFT
FOR TERM
7I47 RS-422 INTERFACE
P1
P2
P3
P4
PTC1
U1
U2
U3
U4
U5
U6
U7
J1
W1
W2
W3
W4
W5
W6
W7
W8
W9
W10
W11
W12
W13
W14
W15
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C12
C13
C14
C15
C16
C17
C20
C21
C22
R1
R2
R3
R5
R23
R25
RN1
RN2
RN3
RN4
TX11
TX10
TX9
TX8
TX7
TX6
TX5
TX4
TX3
TX2
TX1
TX0
RXI3
RXB3
RXA3
RXI2
RXB2
RXA2
RXI1
RXB1
RXA1
RXI0
RXB0
RXA0
+5V
G