7I36 MANUAL

Four channel analog servo amp interface

V1.4

This page intentionally almost blank

Table of Contents

GENERAL

DESCRIPTION

The 7I36 is a 4 axis analog servo interfaces intended for operation with MESA's Anything I/O cards when used for motion control applications.

The 7I36 takes PWM signals from the Anything I/O card and converts them to +-10V analog output voltages for direct connection to analog input servo amplifiers.

Each analog channel has an independent enable with a floating optocoupler output for compatibility with sourcing or sinking drive enable inputs. The 7I36 also conditions the encoder input signals with input buffers for differential encoder signals. Encoder signal wiring integrity data is provided for the A,B, and index signals of all axis.

In addition to the analog and encoder I/O, the 7I36 has 16 isolated 4V to 24V inputs with 2 independent commons allowing sourcing or sinking inputs. 8 of the isolated inputs can be use to support up to 4 MPG encoders.

One RS-422/RS-485 port is provided for I/O expansion using Mesa's SSerial expansion cards.

The controller connection is a 50 pin header that matches the pinout of the Mesa 50 pin anything I/O series of cards. The 7I36 uses Phoenix compatible 3.5 mm headers and is supplied with pluggable terminal blocks.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 7I36 card is oriented in an upright position, that is, with the 50 pin controller connector is on the left hand side,

DEFAULT CONFIGURATION

JUMPER	FUNCTION	DEFAULT SETTING
W1	CABLE POWER SELECT	LEFT = CABLE POWER

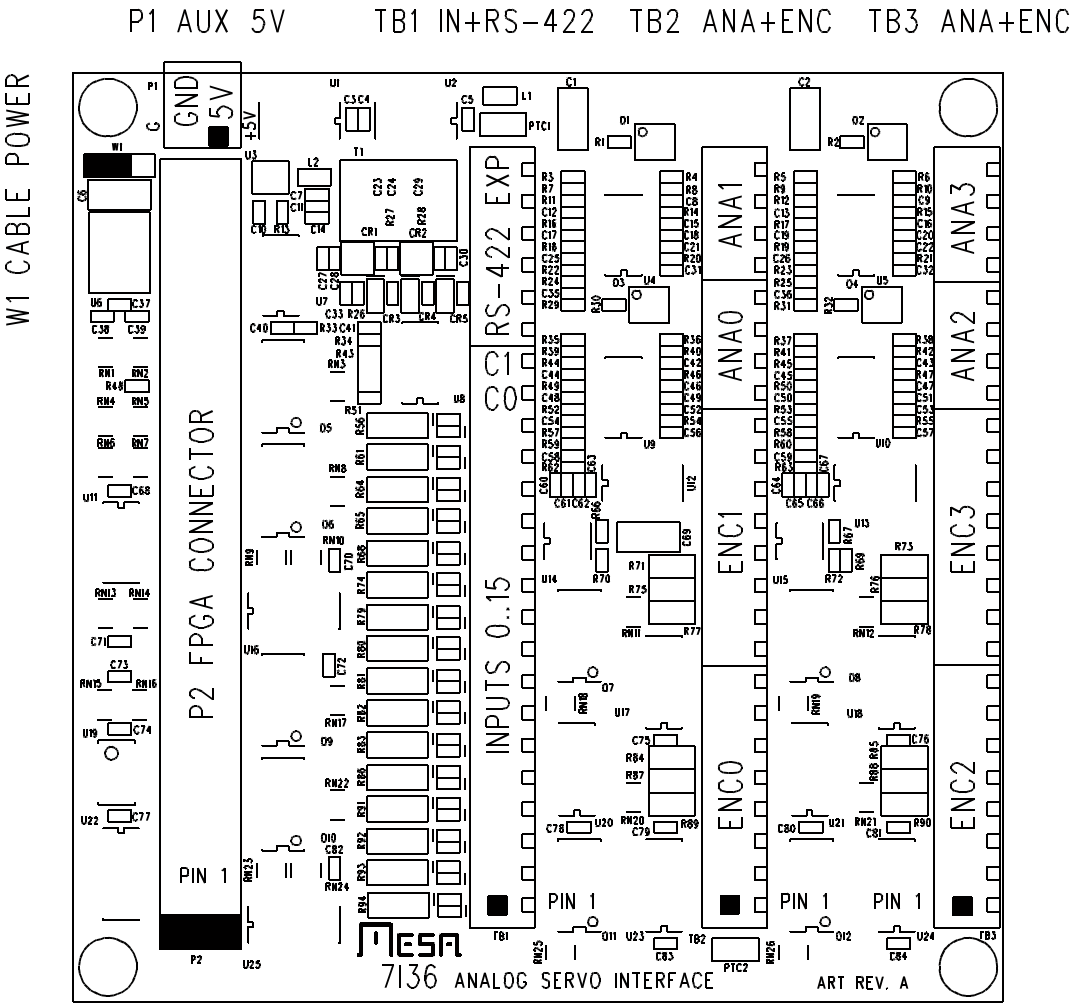
.

CABLE POWER/P1 POWER SELECTION

The 7I36 can get its operating power from the flat FPGA cable or from P1. For testing and with very low power encoders, cable power can be used. W1 selects whether cable power connects to the 7I36s 5V supply. If W1 is in the "RIGHT" position, cable power is selected. If W1 is in the "LEFT" position, external 5V power must be supplied via P1.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITION



CONNECTORS

CONTROLLER CONNECTOR

50 pin header connector J1 connects to the anything I/O card/motion controller. Controller connector pin-out is as follows:

PIN	FUNCTION	DIRECTION	PIN	FUNCTION	DIRECTION
1	MUXIDX1	FROM 7I36	25	/ENA2	TO 7I36
3	MUXQB1	FROM 7I36	27	/PWM2	TO 7I36
5	MUXQA1	FROM 7I36	29	/ENA1	TO 7I36
7	MUXIDX0	FROM 7I36	31	/PWM1	TO 7I36
9	MUXQB0	FROM 7I36	33	/ENA0	TO 7I36
11	MUXQA0	FROM 7I36	35	/PWM0	TO 7I36
13	MUXSEL0	TO 7I36	37	IMUXDATA	FROM 7I36
15	TXEN	TO 7I36	39	IMUXADD4	TO 7I36
17	TXD	TO 7I36	41	IMUXADD3	TO 7I36
19	RXD	FROM 7I36	43	IMUXADD2	TO 7I36
21	/ENA3	TO 7I36	45	IMUXADD1	TO 7I36
23	/PWM3	TO 7I36	47	IMUXADD0	TO 7I36
			49	+5V PWR	TO 7I36

Note: all even pins are grounded.

AUX 5V POWER

The 7I36 can get its 5V power from the FPGA cable or connector P1. Normally P1 should be used for power as the 5V current draw from 4 encoders will exceed what the FPGA flat cable can deliver.

PIN	FUNCTION
1	5V
2	GND

CONNECTORS

ISOLATED INPUT AND SERIAL CONNECTOR

TB1 is the 7I36s isolated input and serial interface connector.

TB1 PIN	SIGNAL	DIRECTION	FUNCTION
1	INPUT0	TO 7I36	ISOLATED INPUT 0
2	INPUT1	TO 7I36	ISOLATED INPUT 1
3	INPUT2	TO 7I36	ISOLATED INPUT 2
4	INPUT3	TO 7I36	ISOLATED INPUT 3
5	INPUT4	TO 7I36	ISOLATED INPUT 4
6	INPUT5	TO 7I36	ISOLATED INPUT 5
7	INPUT6	TO 7I36	ISOLATED INPUT 6
8	INPUT7	TO 7I36	ISOLATED INPUT 7
9	INPUT8	TO 7I36	ISOLATED INPUT 8
10	INPUT9	TO 7I36	ISOLATED INPUT 9
11	INPUT10	TO 7I36	ISOLATED INPUT 10
12	INPUT11	TO 7I36	ISOLATED INPUT 11
13	INPUT12	TO 7I36	ISOLATED INPUT 12
14	INPUT13	TO 7I36	ISOLATED INPUT 13
15	INPUT14	TO 7I36	ISOLATED INPUT 14
16	INPUT15	TO 7I36	ISOLATED INPUT 15
17	INCOM0..7	TO 7I36	COMMON FOR INPUTS 0..7
18	INCOM8..15	TO 7I36	COMMON FOR INPUTS 8..15
19	GND	TO 7I36	SERIAL GND
20	RX+	TO 7I36	SERIAL RECV +
21	RX-	TO 7I36	SERIAL RECV-
22	TX+	FROM 7I36	SERIAL XMIT+
23	TX-	FROM 7I36	SERIAL XMIT-
24	+5VP	FROM 7I36	SERIAL +5 (PTC PROTECTED)

CONNECTORS

SERVO AMP/ENCODER CONNECTORS

The 7I36s servo amplifier / encoder connectors (TB1 and TB2) are 3.5MM 24 pin headers compatible with Phoenix pluggable terminal blocks (supplied with 7I36). Connector TB2 has the I/O signals for channels 0 and 1:

TB2 PIN	SIGNAL	DIRECTION	FUNCTION
1	ENCA0	TO 7I36	ENCODER 0 QUAD A
2	/ENCA0	TO 7I36	ENCODER 0 INVERTED QUAD A
3	GND	FROM 7I36	ENCODER 0 GROUND
4	ENCB0	TO 7I36	ENCODER 0 QUAD B
5	/ENCB0	TO 7I36	ENCODER 0 INVERTED QUAD B
6	+5V	FROM 7I36	ENCODER 0 5V POWER
7	ENCX0	TO 7I36	ENCODER 0 INDEX
8	/ENCZ0	TO 7I36	ENCODER 0 INVERTED INDEX
9	ENCA1	TO 7I36	ENCODER 1 QUAD A
10	/ENCA1	TO 7I36	ENCODER 1 INVERTED QUAD A
11	GND	FROM 7I36	ENCODER 1 GROUND
12	ENCB1	TO 7I36	ENCODER 1 QUAD B
13	/ENCB1	TO 7I36	ENCODER 1 INVERTED QUAD B
14	+5V	FROM 7I36	ENCODER 1 5V POWER
15	ENCX1	TO 7I36	ENCODER 1 INDEX
16	/ENCZ1	TO 7I36	ENCODER 1 INVERTED INDEX
17	GND	FROM 7I36	ANALOG 0 GROUND
18	DRV0	FROM 7I36	ANALOG 0 OUT
19	ENA0-	FROM 7I36	ENABLE 0 OUT-
20	ENA0+	FROM 7I36	ENABLE 0 OUT+
21	GND	FROM 7I36	ANALOG 1 GROUND
22	DRV1	FROM 7I36	ANALOG 1 OUT
23	ENA1-	FROM 7I36	ENABLE 1 OUT-
24	ENA1+	FROM 7I36	ENABLE 1 OUT+

CONNECTORS

SERVO AMP/ENCODER CONNECTORS

Connector TB3 has the I/O signals for channels 2 and 3:

TB3 PIN	SIGNAL	DIRECTION	FUNCTION
1	ENCA2	TO 7I36	ENCODER 2 QUAD A
2	/ENCA2	TO 7I36	ENCODER 2 INVERTED QUAD A
3	GND	FROM 7I36	ENCODER 2 GROUND
4	ENCB2	TO 7I36	ENCODER 2 QUAD B
5	/ENCB2	TO 7I36	ENCODER 2 INVERTED QUAD B
6	+5V	FROM 7I36	ENCODER 2 5V POWER
7	ENCX2	TO 7I36	ENCODER 2 INDEX
8	/ENCZ2	TO 7I36	ENCODER 2 INVERTED INDEX
9	ENCA3	TO 7I36	ENCODER 3 QUAD A
10	/ENCA3	TO 7I36	ENCODER 3 INVERTED QUAD A
11	GND	FROM 7I36	ENCODER 3 GROUND
12	ENCB3	TO 7I36	ENCODER 3 QUAD B
13	/ENCB3	TO 7I36	ENCODER 3 INVERTED QUAD B
14	+5V	FROM 7I36	ENCODER 3 5V POWER
15	ENCZ3	TO 7I36	ENCODER 3 INDEX
16	/ENCZ3	TO 7I36	ENCODER 3 INVERTED INDEX
17	GND	FROM 7I36	ANALOG 2 GROUND
18	DRV2	FROM 7I36	ANALOG 2 OUT
19	ENA2-	FROM 7I36	ENABLE 2 OUT-
20	ENA2+	FROM 7I36	ENABLE 2 OUT+
21	GND	FROM 7I36	ANALOG 3 GROUND
22	DRV3	FROM 7I36	ANALOG 3 OUT
23	ENA3-	FROM 7I36	ENABLE 3 OUT-
24	ENA3+	FROM 7I36	ENABLE 3 OUT+

OPERATION

PWM RATE

The 7I36 is meant to operate with PWM rates from 24 KHz to 48 KHz. Operation at lower PWM rates will result in excessive output ripple, operation at higher PWM rates will result in poor linearity. When used with HostMot2 firmware, the PWM generators should be set for mode 1 with the offset mode flag set true and the PWM frequency set for 48KHz.

STEP RESPONSE

The 7I36 has a 5 pole PWM filter with an approximate 100 uSec time constant. This value is selected as a compromise between output ripple and settling time. This is much faster than most controlled devices so will not normally have any effect on loop stability or performance.

ENCODER INPUT CIRCUIT

The 7I36 encoder input circuits accept differential mode encoder signals. In addition, the inputs detect wiring integrity by sensing that a valid differential signal is present on the A,B and index inputs.

MAXIMUM COUNT RATE

The 7I36 uses multiplexed encoder signals to save interface pins. The multiplexing rate will determine the maximum encoder count rate. Default multiplexing rate with HostMot2 firmware is ClockLow / 8, or approximately 4 or 6 MHz, giving a resolvable count rate of 2 to 3 MHz. Multiplexing rate can be increased if desired but high multiplex rates will require short cables between the FPGA controller card and the 7I36 due to signal integrity and time-of-flight considerations. Maximum practical multiplex rate is approximately 12 MHz (and 6 MHz count rates). Encoder count rate is further limited by HostMot2s input filtering to ~5 to ~8 million counts per second (encoder filtering off) and ~1 to ~1.6 million counts per second (encoder filtering on).

OPERATION

5V POWER

The 7I36 requires ~400 mA of 5V power for operation. Encoder power can also be supplied from the 7I36's 5V source. Power for the 7I36 is normally supplied from P1 but can also be supplied via pin 49 of the 50 conductor controller cable when testing or when low power encoders are used.

ENABLE INPUTS

Each analog output channel uses a separate enable. These enables are active low at the FPGA interface. When an enable is high the enable output is off and the analog output voltage is set to 0V. Pullup resistors keep the enable inputs high if the controller connection is lost.

ENABLE OUTPUTS

Each 7I36 channel has a OPTO-isolated transistor output that can be used to enable external amplifiers. Maximum switched voltage is 36VDC. Maximum output current is 10 mA. All are isolated to allow different enable connections on a per amplifier basis.

Example connections:

1. Active high +12V amplifier enable on channel 0:

    Connect ENA0+ to +12V source

    Connect ENA0- to amplifier enable input

2. Active low TTL input on channel 2

    Connect ENA2- to ground

    Connect ENA2+ to amplifier enable input

ANALOG OUTPUTS

The analog output of the 7I36 swings from -10 v to +10V. Positive outputs are generated when the PWM has a less than 50% duty cycle and negative outputs are generated when PWM has a greater than 50% duty cycle. Because of thi,s the PWM output should be inverted if positive PWM values are to generate positive voltages and negative outputs when PWM- is driven. A 50 % duty cycle PWM signal will generate a 5V output. This mode of operation requires the PWM generator be set for offset mode. *Due to power supply limitations, The 7I36 has limited DC output drive capability and should not have loads of less than 3K Ohms on its analog outputs. (~24 mA maximum total +-10v current). To avoid power supply damage, do no short more than one analog output at once*.

OPERATION

ISOLATED INPUTS

The 7I36 provides 16 isolated inputs for general purpose use on TB1. These inputs are optically isolated and can be used with 4V to 24V input signal levels. The inputs are divided into two groups of 8 inputs: Inputs 0..7 and inputs 8..15. Each group has a separate common. The separate commons mean that the inputs can be used for sinking (common ground for PNP type sensors), sourcing (common V+ for NPN type sensors), or combinations of both. With standard FPGA firmware, Inputs 0..7 can be used to support up to 4 MPG encoders.

ENCODER SIGNAL INTEGRITY

All encoder input signals are monitored for signal strength to determine wiring integrity. A high bit indicates a valid encoder input signal. Inmux input bits 0..15 are used for the general purpose isolated inputs and inmux inputs 16..31 are used for encoder signal status. Bits 19,23,27,31 will read high in normal operation.

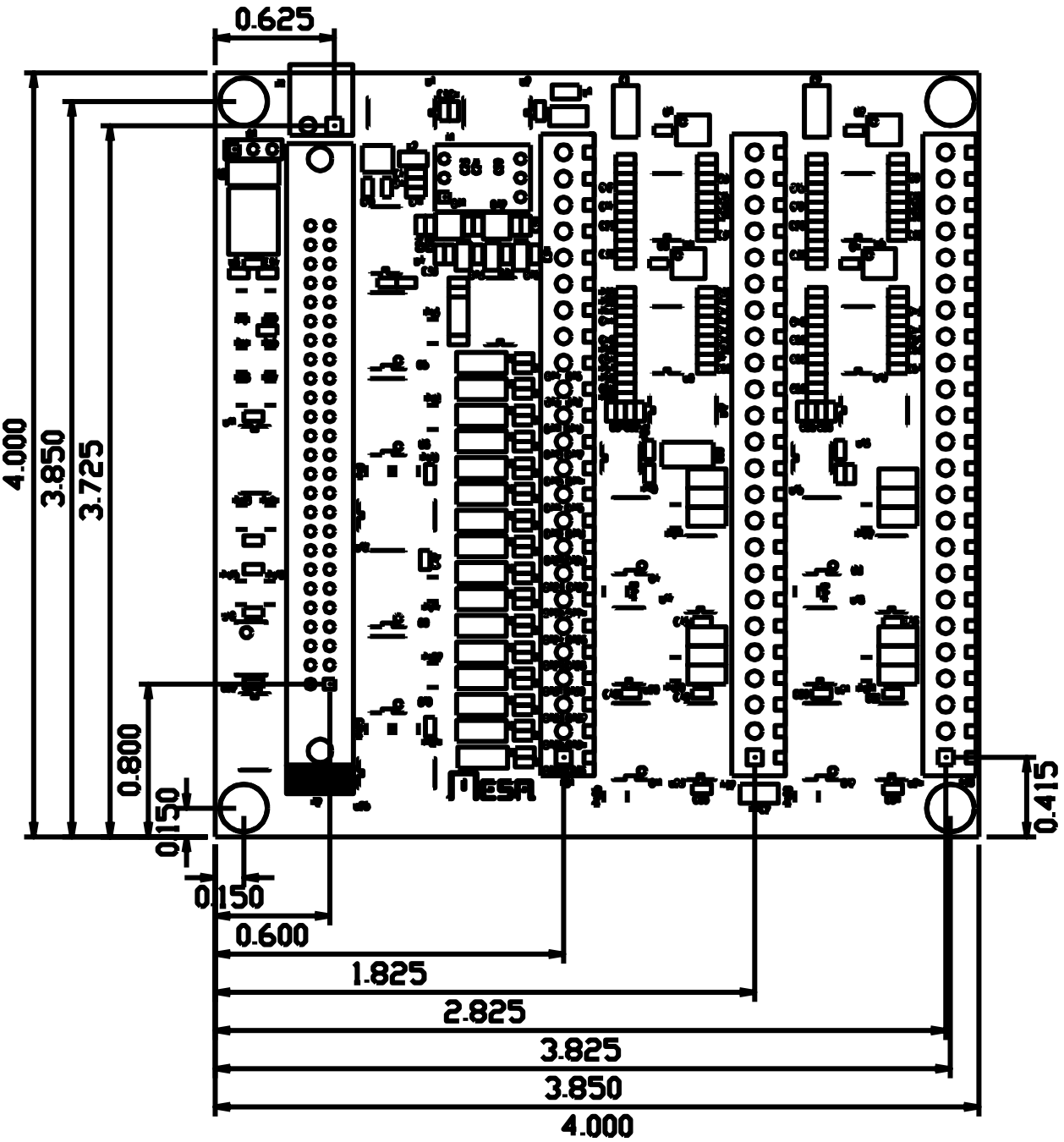
ENCODER STATUS BITS

INMUX BIT	MONITORED SIGNAL
16	ENCZ0
17	ENCB0
18	ENCA0
19	ALWAYS HIGH
20	ENCZ1
21	ENCB1
22	ENCA1
23	ALWAYS HIGH
24	ENCZ2
25	ENCB2
26	ENCA2
27	ALWAYS HIGH
28	ENCZ3
29	ENCB3
30	ENCA3
31	ALWAYS HIGH

SPECIFICATIONS

	MIN	MAX	UNITS
5V POWER SUPPLY	4.75	5.25	VDC
5V POWER CONSUMPTION (no external load)	---	500	mA
ENCODER			
DIFF VOLTAGE FOR VALID STATUS	1.7	—	V
DIFF VOLTAGE FOR VALID COUNT	200	—	mV
COMMON MODE RANGE	-7	+12	V
ABSOLUTE MAX COMMON MODE	-25	+25	V
ANALOG			
ANALOG OUTPUT VOLTAGE	+-9.8	+-10.2	V
ANALOG OUTPUT STEP RESPONSE	90	110	uSec
MINIMUM AOUT LOAD RESISTANCE	3K	---	Ohm
OUTPUT RIPPLE @ 48 KHZ PWM	---	.05%	% FS
LINEARITY	---	.05%	% FS
ZERO OFFSET ERROR	-10	+10	mV
OPERATING TEMP.	0	+70	^{o}C
OPERATING TEMP. (-I version)	-40	+85	^{o}C
OPERATION HUMIDITY	0	95%	NON-COND

DRAWINGS


0.625
4.000
3.850
3.725
0.800
0.150
0.150
0.600
1.825
2.825
3.825
3.850
4.000
0.415