4I30 QUADRATURE COUNTER MANUAL

VERSION 1.2

nm

Mesa Electronics
4175 Lakeside Drive, Suite #100
Richmond, CA 94806-1950
Tel (510) 223-9272 - Fax (510) 223-9585
E-Mail: tech@mesanet.com - Website: www.mesanet.com

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HANDLING PRECAUTIONS

STATIC ELECTRICITY

The CMOS integrated circuits on the 4I30 can be damaged by exposure to electrostatic discharges. The following precautions should be taken when handling the 4I30 to prevent possible damage.

A. Leave the 4I30 in its antistatic bag until needed.

B. All work should be performed at an antistatic workstation.

C. Ground equipment into which 4I30 will be installed.

D. Ground handling personnel with conductive bracelet through 1 megohm resistor to ground

E. Avoid wearing synthetic fabrics, particularly Nylon.

INTRODUCTION

GENERAL

The MESA 4I30 is a stackable PC/104 card with four 32 bit up/down counters with quadrature count inputs and per channel index inputs. The 4I30 is intended for robotic, motor control, measurement, and instrumentation applications.

The 4I30 has selectable TTL or RS-422 levels on its quadrature and index inputs. TTL or RS-422 operation is jumper selectable in groups of two channels. The TTL inputs have pullup resistors and RC / Schmitt filtering. The differential RS-422 inputs are suited for longer cable lengths and have optional termination. Each time a logic transition occurs at one of the quadrature inputs, the count is incremented or decremented, providing a resolution of four times the line count of the encoder used.

The 4I30 counters may cleared individually, or all counters may be cleared simultaneously. Each counter has a separate programmable count enable/disable with external index input. The 4I30 can be programmed so that the count is synchronized with the external index signal. Index signal polarity is jumper selectable.

Maximum count rate of the 4I30 is 1.5 million counts per second. Count range is -214748368 to +214748367 or 0 to 4,294,967,295. One counter may be configured to provide a timing reference for velocity calculations instead of quadrature input. This timing reference is a 32 bit up counter running at 500 KHz +- .01%.

The 4I30 uses a 50 pin header for I/O connections. The encoder inputs are arranged in groups of 10 pins per encoder. Each 10 pin group includes power and multiple grounds. 5V power on the I/O connectors is fused on the 4I30.

All 4I30 models can use the 16 bit stack through type PC/104 bus architecture. Four layer circuit card construction is used to minimize radiated EMI and provide optimum ground and power integrity. The 4I30 requires only +5V for operation

The 4I30 base address is set with jumpers, and can be located at four separate I/O locations within the 1024 byte I/O address space of the PC/104 bus. Up to four 4I30 cards may be used in a system.

CONFIGURATION

GENERAL

The 4I30 port address and various other options are set with jumpers. Each group of jumpers will be discussed separately by function. In the following discussions, when the words "up", "down", "right", and "left" are used it is assumed that the 4I30 I/O card is oriented with its bus connectors J1 and J2 at the bottom edge of the card (nearest the person doing the configuration).

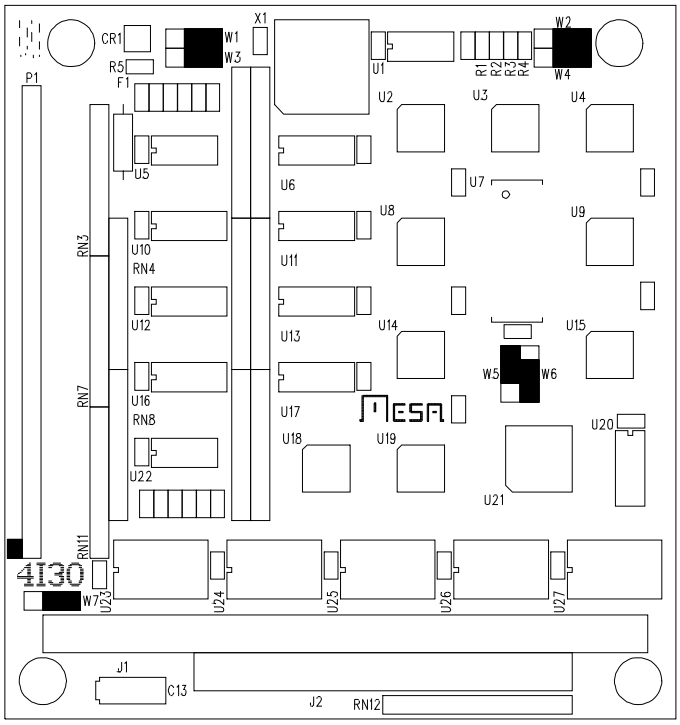
DEFAULT JUMPER SETTINGS

Factory default 4I30 jumpering is as follows:

FUNCTION	JUMPER(S)	SETTING
4I30 Base address	W5,W6	up ,down - 0210H
Input type	W1,W3	right, right -TTL type inputs
Chan 3 timer option	W2	right - Not enabled
Index polarity	W7	right - Active low
Clock option	W4	right - Not implemented

CONFIGURATION

DEFAULT JUMPER SETTINGS



CONFIGURATION

BASE ADDRESS SELECTION

The base I/O address of the 4I30 is selected by placing shorting jumpers on jumper blocks W5 and W6. Jumper blocks W5 and W6 have three pins and two valid shorting jumper locations, up, and down. The following table shows the base address settings:

BASE ADDRESS	W5	W6
0200H	down	down
0208H	down	up
0210H (Default)	up	down
0218H	up	up

INPUT LEVEL SELECTION

Jumpers W1 and W3 select TTL or RS-422 levels on the quadrature and index inputs. W1 selects the input option for channels 2 and 3 while W3 selects the input option for channels 0 and 1. When W1 or W3 are in the right hand position, TTL input levels are selected. When W1 or W3 are in the left hand position, RS-422 levels are selected. Input levels for counter pairs 0-1 and 2-3 can be selected independently, allowing a mix of encoder types.

TIMER OPTION

To facilitate velocity calculations, counter 3 may be configured to provide a timing reference instead of quadrature input. This timing reference is a 32 bit up counter running at 500 KHz +- .01%.

To select this timing reference W2 is placed in the left hand position. If W2 is placed in the right hand position, counter 3 functions as a the quadrature counter.

INDEX POLARITY SELECTION

Polarity of the index signals are selected by W7. When W7 is in the right hand position index levels are active low. When W7 is in the left hand position index levels are active high.

RS-422 TERMINATION

The RS-422 differential inputs are normally always terminated. If termination is not desired resistor networks RN3, RN7, and RN11 may be unplugged.

COUNTER SIZE OPTION

The counter word size option is not yet implemented and W4 must be placed in the right hand position.

INSTALLATION

GENERAL

When the 4I30 has been properly configured for its application, it can be inserted into a PC/104 stack. The standoffs should then be tightened to secure the 4I30 in its place. When the 4I30 is secured in the stack the I/O connectors can be plugged in from the side.

I/O CONNECTOR ORIENTATION

The 50 pin connector on the 4I30 have their pin one ends marked with a white square on the circuit card. This is at the bottom (near the PC/104 connectors). (Note: Some early cards have pin one mismarked. See page 7 for correct location). This corresponds with the red stripe on typical flat cable assemblies. If more positive polarization is desired, center polarized IDC header connectors should be used. These connectors will not fully mate with the pins on the 4I30 if installed backwards. A suggested center polarized 50 pin IDC header is AMP PN 1-746285-0.

The connections to each encoder is a group of 10 pins. These 10 pin groups can be split off from the 50 conductor flat cable and individually terminated with 10 pin headers.

OPERATION

CONNECTOR PIN-OUT

The 4I30 50 pin I/O connector pinout is as follows:

P1 CONNECTOR

PIN	**SIGNAL**	**PIN**	**SIGNAL**
1	ENCA0	2	/ENCA0
3	GND	4	ENCB0
5	/ENCB0	6	GND
7	IDX0	8	/IDX0
9	GND	10	+5V Fused power
11	ENCA1	12	/ENCA1
13	GND	14	ENCB1
15	/ENCB1	16	GND
17	IDX1	18	/IDX1
19	GND	20	+5V Fused power
21	ENCA2	22	/ENCA2
23	GND	24	ENCB2
25	/ENCB2	26	GND
27	IDX2	28	/IDX2
29	GND	30	+5V Fused power
31	ENCA3	32	/ENCA3
33	GND	34	ENCB3
35	/ENCB3	36	GND
37	IDX3	38	/IDX3
39	GND	40	+5V Fused power
41	GND	42	GND
43	GND	44	GND
45	GND	46	+5V Fused power
47	+5V Fused power	48	+5V Fused power
49	+5V Fused power	50	+5V Fused power

OPERATION

ENCODER POWER

The 4I30 can supply +5V to power external encoders or other external devices. If these external devices are powered remotely do not connect to the +5V on the 4I30. +5V power on the 4I30 is fused. Note that the +5V fuse is rated at 1 Amp and can be replaced without soldering. Replacement part number is LittleFuse PN 250001.

CONNECTING TTL ENCODERS

When using TTL output encoders, select the TTL input type for the counter using W1 and W3. Connect the "A" output of the encoder to /ENCAn, the "B" output to /ENCBn, and the "I" output to /IDXn (where n is the counter number). As an alternative, if the terminator resistors are installed (RN3, RN7, RN11), the active high input can also be used. Nominal input filter time constant on the 4I30 TTL inputs is 220 nS. If it is desired to increase the R/C time constant, a higher value of terminator resistor can be substituted.

CONNECTING OPEN COLLECTOR ENCODERS

When using open collector output encoders connect for TTL input as above. A 3.3K pullup resistor is provided. If this value is not suitable the resistor networks RN4 and RN8 may be replaced with an appropriate value. RN8 is the pullup for channel 0 and 1, RN4 is the pullup for channels 2 and 3. The pullup resistor networks are 10 pin SIP's 9 resistor with pin 1 common. Pin one points down.

CONNECTING RS-422 ENCODERS

When using RS-422 output encoders select the RS-422 input type for the counter using W1 and W3. Connect the "\A" output of the encoder to /ENCAx, the "A" output of the encoder to ENCAx, the "/B" output to /ENCBx", the B",output to ENCBx, the "/I" output to /IDXx, and the "/I" output to /IDXx (where x is the counter number). If termination is not desired remove RN3, RN7, and RN11.

ENCODER DIRECTION

If it is desired to reverse the count direction on a particular channel, interchange the A and B signals.

OPERATION

REGISTER MAP

The I/O registers on the 4I30 occupies 8 contiguous bytes. These 8 bytes start at the I/O address set by jumpers W5 and W6.

ADDRESS	READ DATA	WRITE DATA
BASE +0	Latched counter bits [0..7]	XXXXXXXX
BASE +1	Latched counter bits [8..15]	XXXXXXXX
BASE +2	Latched counter bits [16..23]	XXXXXXXX
BASE +3	Latched counter bits [24..31]	XXXXXXXX
BASE +4	Enable register	Enable register
BASE +5	Index register	XXXXXXXX
BASE +6	Enable register	Command register
BASE +7	Index register	XXXXXXXX

COMMAND REGISTER

All access to the 4I30 counters is done by first writing a command byte to the command register. The command register is located at the 4I30 base address + 6. When the command byte is written, the busy bit is set, indicating that the command is being executed. This applies to all clear and read counter commands. When the busy bit is clear, the operation is complete. The typical time to complete a command is 3 uS. The maximum time is 4 uS. After issuing a command, interface software can poll the busy bit to determine when the requested operation is complete, or wait 4 uS after the command before issuing another command or reading a counter.

Commands that access individual counters specify the counter with the 2 least significant bits of the command register.

COMMAND REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BSY	XXX	LED	CLRA	CLR	READ	SEL1	SEL0

OPERATION

4I30 COMMANDS

These are the valid command bytes in hex:

COMMAND	COMMAND BYTE
READ COUNTER 0	84H
READ COUNTER 1	85H
READ COUNTER 2	86H
READ COUNTER 3	87H
CLEAR COUNTER 0	88H
CLEAR COUNTER 1	89H
CLEAR COUNTER 2	8AH
CLEAR COUNTER 3	8BH
CLEAR ALL	90H
LED ON	20H
LED OFF	00H

BUSY BIT

Once a command is written, interface software can poll the busy bit in the status register to determine when the command is complete. The busy bit is bit 7 at register offsets 4,5,6 and 7. All commands that have the BSY bit set take between 2 and 4 uS to complete.

READING A COUNTER

The sequence of events for reading counter 0 is as follows:

1. Issue the READ COUNTER 0 command (Write 84H to 4I30 address +6)
2. Wait for busy bit to be clear (Poll bit 7 of 4I30 address +6 until low)
3. Read latched counter data (Read bytes from 4I30 address +0,+1,+2, +3)

Successive bytes of the 32 bit count value are located at successive I/O locations. This makes it possible to read the counter as four individual bytes, two 16 bit words, or a single 32 bit value (386 processors and above) using four, two, or a single input instruction. When reading counters, the latched data will remain valid until the next read counter command is issued.

OPERATION

INDEX OPERATION

It is possible to synchronize each counter on the 4I30 with an external index input. Each counter channel has an associated count enable bit. These bits can be set and cleared by software, and set by the external index inputs. By initially clearing an enable bit, and clearing the associated counter, the counter is 'primed' such that it will begin counting when the index input becomes active and both input phases are 0. *Software cannot clear the enable flip flops if the index input is active.* Once the counter is enabled, further changes in the index input have no effect. Both the enable flip flop and the real time index input status can be read from the 4I30.

ENABLE REGISTER

The enable bits are accessible at 4I30 base address + 4. The enable register is a 4 bit, read-write register. The BSY bit is a read only bit in the enable register.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BSY	XXX	XXX	XXX	ENA3	ENA2	ENA1	ENA0

Setting an enable bit high enables counting on the associated counter. Setting an enable bit low disables counting. When counting is enabled, the quadrature decoder circuitry waits until both input phases are low before starting to count. The enable inputs are unconditionally set by active index inputs.

If the associated index inputs are inactive, counting can be enabled and disabled under software control by setting or clearing the appropriate enable bits.

NOTE: There is a BUG in the current hardware for the enable register that makes writes fail occasionally. To write data to the enable register you must write the data, and read back the enable register and retry until the desired bits are set.

INDEX STATUS REGISTER

The real time status of the index inputs can be read at 4I30 base address + 5. The IDX bits are always high true regardless of the index polarity jumper setting. A high bit means that the index is active.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BSY	XXX	XXX	XXX	IDX3	IDX2	IDX1	IDX0

OPERATION

USING THE INDEX INPUTS

Quadrature encoders are *relative* angle or distance measuring devices. Any system that needs absolute position measurement with quadrature encoders requires some kind of absolute position reference. Some rotary encoders have a once per rotation index output. Linear encoders often have a zero position reference signal. These reference signals can be used to synchronize the quadrature counter with absolute angle or position . This is usually done at system power-up.

To use the 4I30 index inputs, you need to set the index polarity such that the normal index level is inactive. On system start-up you need to ensure that the index input is inactive (by polling the index status register of the 4I30 and moving the measured device if necessary). When the index is inactive you disable counting by writing a zero to the appropriate bit of the enable register. You then clear the quadrature counter. Now the measured device is moved until the index signal becomes active. At this point the quadrature counters are enabled, and will remain enabled regardless of further changes in the index input.

By using this procedure, the inactive - active transition of the index input effectively become the zero count reference point.

A FINE POINT

When counting has been disabled and the re-enabled, the quadrature decoder does not begin counting until the 0,0 input state is present. This is to allow some 'slop' in the index position detection on the encoder. The reference position is quantized to a 4 count interval meaning that the position accuracy of the system is based on the quadrature signals, not the less accurate index signal.

TIMING REFERENCE

4I30 counter 3 can be used as a time base for velocity measurement if desired. If W2 is set to the left hand position, counter 3 no longer responds to the quadrature inputs, but simply counts up at 500 KHz. This frequency is crystal controlled and accurate to .01%. The procedure for reading and clearing the counter are the same. When counter 3 is used as a timing reference, enable bit 3 and index input 3 have no effect on the count.

MAXIMUM COUNT RATE

The 4I30 can count quadrature encoder inputs at up to 1.5 million edges per second. This is a hard limit, determined by the 4I30 counter state machine and its crystal clock. Input rates above 1.5 million counts per second will cause the 4I30 to lose counts, such that the maximum observed count rate will remain at 1.5 million per second. That is, the count rate is bounded at 1.5 million counts per second.

REFERENCE INFORMATION

SPECIFICATIONS

	MIN	MAX	UNIT	NOTES
POWER SUPPLY				
Voltage	4.5	5.5	V	
Supply current (5V)	---	500	mA	
BUS LOADING:				
Input capacitance	---	15	pF	
Input leakage current	---	5	uA	
Output drive capability	150	---	pF	
Output sink current	12	---	mA	
INPUTS:				
TTL input current	1.3	1.7	mA	3.3K pullups
RS-422 input sensitivity	---	200	mV	Differential
ENVIRONMENTAL:				
Operating temperature range				
-I version	-40	+85	°C	
-C version	0	+70	°C	
Relative humidity	0	90	Percent	Non-condensing

REFERENCE INFORMATION

WARRANTY

Mesa Electronics warrants the products it manufactures to be free effects in material and workmanship under normal use and service for the period of 2 years from date of purchase. This warranty shall not apply to products which have been subject to misuse, neglect, accident, or abnormal conditions of operation.

In the event of failure of a product covered by this warranty, Mesa Electronics, will repair any product returned to Mesa Electronics within 2 years of original purchase, provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may at its option, replace the product in lieu of repair.

With regard to any product returned within 2 years of purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions of operation, repairs will be billed at a nominal cost.

THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED. INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS, OR ADEQUACY FOR ANY PARTICULAR PURPOSE OR USE. MESA ELECTRONICS SHALL NOT BE LIABLE FOR ANY SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER IN CONTRACT, TORT, OR OTHERWISE.

If any failure occurs, the following steps should be taken:

1. Notify Mesa Electronics, giving full details of the difficulty. On receipt of this information, service data, or shipping instructions will be forwarded to you.

2. On receipt of the shipping instructions, forward the product, in its original protective packaging, transportation prepaid to Mesa Electronics. Repairs will be made at Mesa Electronics and the product returned transportation prepaid.

REFERENCE INFORMATION

SCHEMATICS